Siemens EDA

2020 Wilson Research Group functional verification study

IC/ASIC functional verification trend report

Executive summary

This report presents the results from the 2020 Wilson Research Group functional verification study, which were focused on the integrated circuit (IC) and application specific integrated circuit (ASIC) market segments. The findings from this study provide invaluable insight into the state of today's IC/ASIC market in terms of both design and verification trends.

Harry Foster

Contents

I. Introduction

This report presents integrated circuit (IC) and application specific integrated circuit (ASIC) functional verification trends based on the 2020 Wilson Research Group functional verification study, which is a continuation of a series of industry studies that have occurred over the past eighteen years.[1, 2, 3, 4, 5, 6] For our 2020 study, we have separated FPGA from IC/ASIC functional verification trends, and this report focuses on the latter.

A. The global IC/ASIC semiconductor market

The 2019 global semiconductor market was valued at $385.4 billion after experiencing a 15 percent decline due to a 32 percent drop in the memory IC market, which is expected to recover in 2021. The IC/ASIC portion of the semiconductor market is valued at about $186.6 billion.[7, 8] The IC/ASIC semiconductor market is expected to reach a value of $233.4 billion by 2024, growing at a compounded annual growth rate (CAGR) of 4.6 percent during this forecast period. While COVID-19 has had a negative impact in 2020 on a number of market segments (e.g., consumer and automotive), other market segments (e.g., data center computing, networking, storage, and communication) are experiencing positive growth required to support today's growing work-from-home (WFH) environment.

B. Study background

The study results presented in this report are a continuation of a series of industry studies on functional verification. This series includes the previously published 2012, 2014, 2016, and 2018 Wilson Research Group functional verification study.[3, 4, 5, 6] Each of these studies was modeled after the 2002 and 2004 Collett International Research, Inc. studies[1, 2] and focus on the IC/ASIC market.

For the purpose of our study, a randomized sampling frame was constructed from multiple acquired industry lists. This enabled us to cover all regions of the world and all relevant electronics industry market segments. It is important to note that we did not include our own account team's customer list in the sampling frame. This was done in a deliberate attempt to prevent vendor bias in the final results. While we architected the study in terms of questions and then compiled and analyzed the final results, we commissioned Wilson Research Group to execute our study. After data cleaning the results to remove inconsistent, incomplete, or random responses, the final sample size consisted of 1492 eligible participants (i.e., n=1492).

Fig. 1 compares the percentage of 2020 and 2018 study participants (i.e., design projects) by targeted implementation for both IC/ASIC and FPGA projects.

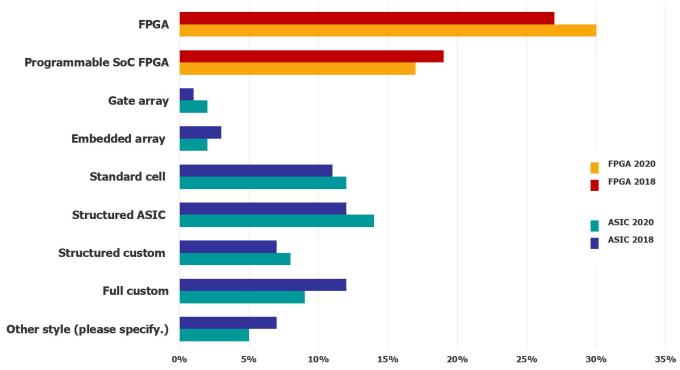

Fig. 1: Study participants by targeted implementation.

C. Study confidence interval

Since all survey-based studies are subject to sampling errors, we attempt to quantify this error in probabilistic terms by calculating a confidence interval. For our study, we determined the overall margin of error to be ±3 percent using a 95 percent confidence interval. In other words, this confidence interval tells us that if we were to take repeated samples from a population, 95 percent of the samples would fall inside our margin of error ±3 percent, and only 5 percent of the samples would fall outside.

D. Study bias

When architecting a study, three main bias concerns must be addressed to ensure valid results: sample validity bias, non-response bias, and stakeholder bias. We have adopted multiple techniques to minimize these biases. However, the 2020 study demographics, as shown in fig. 2, saw an 11 percentage points decline in

participation from North America but an increase in participation from Europe and India. This raises some interesting questions. Was the decline in North American participation due to COVID-19, which was peaking in the US during the June-July timeframe, as many employees shifted their work routine to a home environment? Or were spam filters more aggressive than in previous years, preventing the invitation from reaching potential study participants? Regardless, the shift in balance in the study demographics can introduce potential non-response biases in the findings that need to be considered. For example, regional shifts in participation can influence the findings for design and verification language adoption trends. Potential biases in the data will be highlighted when appropriate.

E. Report organization

The remainder of this report is organized as follows. In Section II, we discuss the study findings related to IC/ASIC verification effectiveness. In Section III, we discuss trends in terms of IC/ASIC project resources. In Section IV, we discuss the study results specifically related to various aspects of IC/ASIC design to illustrate growing complexity. In Section V, we examine IC/ASIC verification technology adoption trends. In addition, this section presents adoption trends for various design and verification language and methodology standards. Then in Section VI, we discuss emulation and FPGA prototyping trends. Finally, in Section VII, we draw some conclusions and discuss various aspects from this year's study.

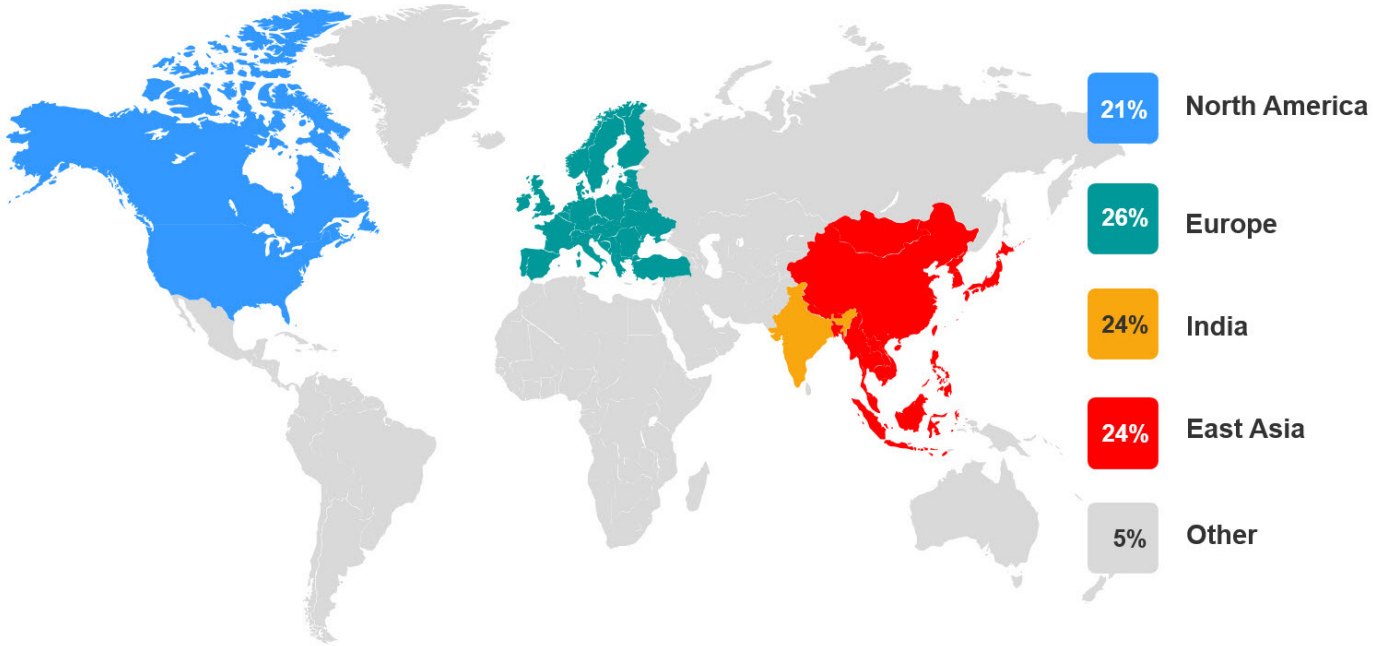

Fig. 2: 2020 study demographics.

II. IC/ASIC verification effectiveness

In this section, we present IC/ASIC project results in terms of verification effectiveness.

A. Required spins

Fig. 3 presents industry trends from 2012 through 2020 in terms of required spins before production. Even though designs have increased in complexity during this period, the data suggest that the number of required spins before production has not increased. Nonetheless, only about 32 percent of today's projects are able to achieve first silicon success.

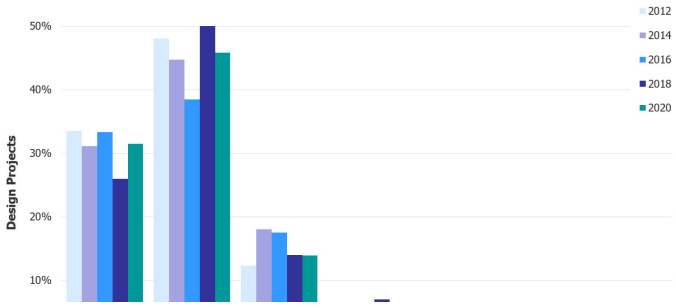

Fig. 3: IC/ASIC spins required before production.

B. Types of flaws resulting in respins

Fig. 4 shows various categories of design flaws contributing to IC/ASIC respins. The percentage of "logic or functional flaws" remains the leading cause of bugs, although in 2020 we saw a huge increase in flaws attributed to tuning analog circuits (41 percent), which warrants additional investigation.

In 2020 we began tracking flaws associated with safety (11 percent) and security (10 percent) features. Obviously multiple flaws can contribute to bug escapes, which is the reason the total percentage of flaws sums to more than 100 percent.

Fig. 5 demonstrates the root cause of logical or functional flaws by various categories. The data suggest design errors are the leading cause of functional flaws, and the situation is worsening. In addition, problems associated with changing, incorrect, and incomplete specifications are a common theme often voiced by many verification engineers and project managers.

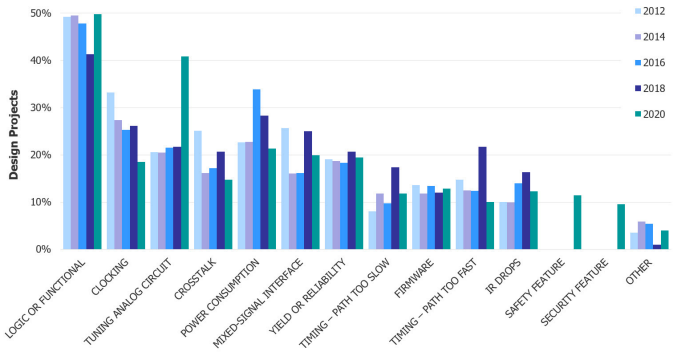

Fig. 4: Types of flaws resulting in IC/ASIC bug escapes.

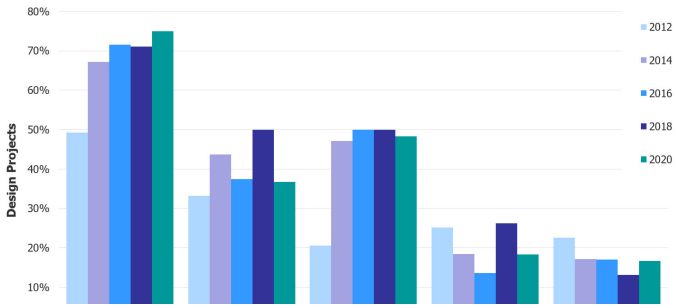

Fig. 5: Root cause of functional flaws.

C. Design completion compared to original schedule

In addition to bug escape metrics that we used to determine an IC/ASIC project's effectiveness, another metric we tracked was project completion compared to the original schedule, as shown in fig. 6. Here we found that 68 percent of IC/ASIC projects were behind schedule.

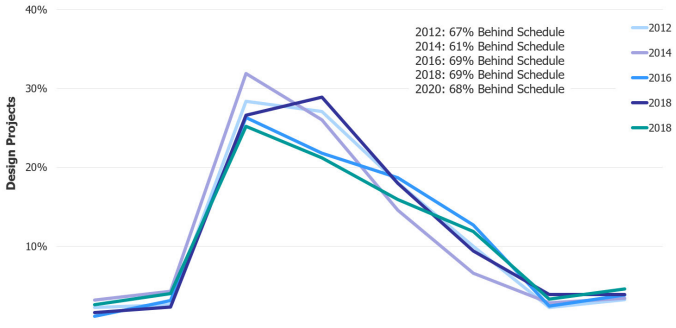

Fig. 6: Actual IC/ASIC project completion compared to original schedule.

III. IC/ASIC verification effort

In this section, we discuss trends in terms of IC/ASIC project time and resources.

A. Percentage of project time spent in verification

Fig. 7 shows the percentage of total IC/ASIC project time spent in verification. You can see two extremes in this graph. In general, projects that spend very little time in verification are typically working on designs with a good deal of existing pre-verified design IP, which is integrated to create a new product. On the other extreme, projects that spend a significant amount of time in verification often have a high percentage of newly developed design IP that must be verified.

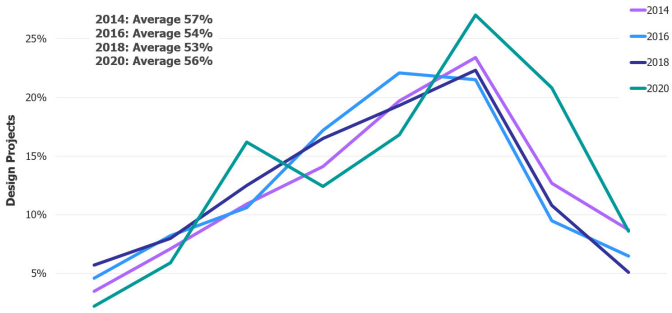

Fig. 7: Percentage of IC/ASIC project time spent in verification.

Notice the increase in project times greater than 60 percent for this year's study. Again, this is a potential indication of growing design and verification complexity.

B. Mean peak number of engineers

Perhaps one of the biggest challenges today is to control cost and engineering headcount, which means identifying IC/ASIC design and verification solutions that increase productivity. To illustrate the need for productivity improvement, we discuss the trend in terms of increasing engineering headcount. Fig. 8 shows the mean peak number of IC/ASIC engineers working on a project.

While, on average, the demand for IC/ASIC design engineers grew at about a 3 percent CAGR between 2007 and 2020, the demand for IC/ASIC verification engineers grew at a 6.8 percent CAGR. Today, on average, across all market segments, we find about a one-to-one ratio in terms of mean peak number of verification and design engineers. However, in some market segments, such as processors, it is not unusual to find a 5-to-1 ratio.

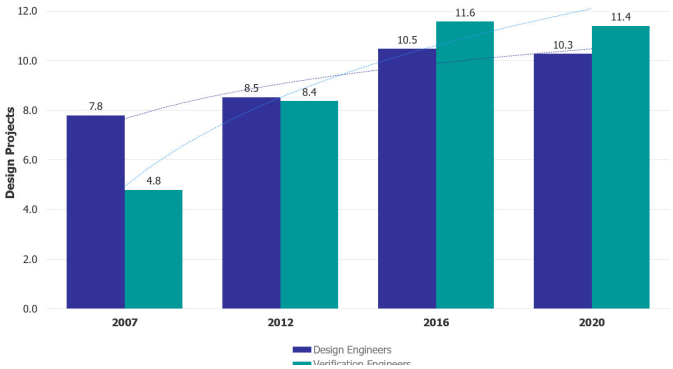

Fig. 8: Mean peak number of IC/ASIC engineers.

But verification engineers are not the only project stakeholders involved in the verification process. Design engineers spend a significant amount of their time in verification too, as shown in fig. 9.

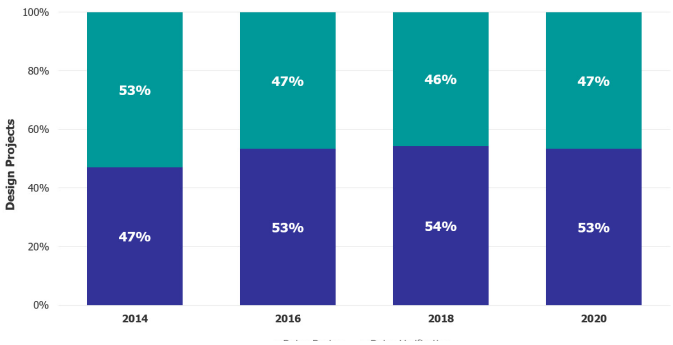

Fig. 9: Where IC/ASIC design engineers spend their time.

In 2020, design engineers spent on average 53 percent of their time involved in design activities and 47 percent of their time in verification. However, when compared to 2014, the data indicate a trend showing that IC/ASIC design engineers are now spending slightly less time involved in verification tasks. There are two reasons for this trend.

Fig. 10 shows where verification engineers spend their time (on average) for various task. Our study found that IC/ASIC verification engineers spend more of their time debugging than with any other activity. From a management perspective, this can be a significant challenge when planning future projects' effort and schedule based on previous projects' data since debugging is unpredictable and varies significantly between projects.

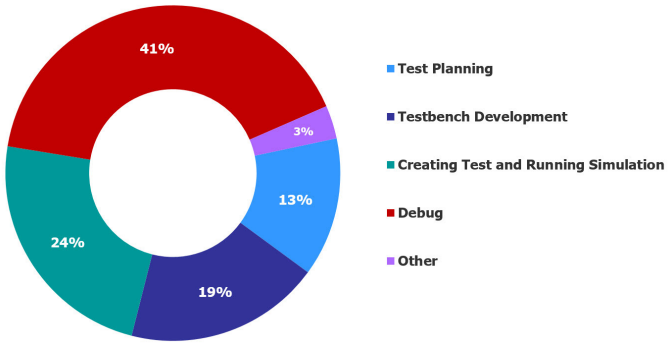

Fig. 10: Where IC/ASIC verification engineers spend their time.

IV. IC/ASIC design trends

One industry driver that has had a substantial impact on IC/ASIC design and verification complexity is the emergence of new layers of design requirements (beyond basic functionality), which did not exist years ago, for example, clocking requirements, security requirements, safety requirements, and requirements associated with hardware-software interactions. In this section, we examine trends related to various aspects of the growing IC/ASIC design complexity.

A. Embedded processor cores

What has changed significantly in IC/ASIC designs in the last twenty years is the movement toward SoC-class designs. For example, our study found that 68 percent of all projects targeted their design at an IC/ASIC containing one or more embedded processors, as shown in fig. 11. Furthermore, 48 percent of all IC/ASIC designs today contain two or more embedded processors, while 17 percent include eight or more embedded processors.

SoC-class designs add a new layer of verification complexity to the verification process[9] that did not exist with traditional non-SoC class designs due to an increased number of design requirements. For example, SoC-class designs often require verification of hardware and software interactions, new coherency architectures, and complex network-on-a-chip interconnect.

Our 2020 study, for the first time, tracked the number of IC/ASIC projects that have incorporated a RISC-V processor in their design, which was 23 percent. In addition, we tracked the number of IC/ASIC projects that have incorporated some type of AI accelerator processor (e.g., TPU, etc.), which was 27 percent.

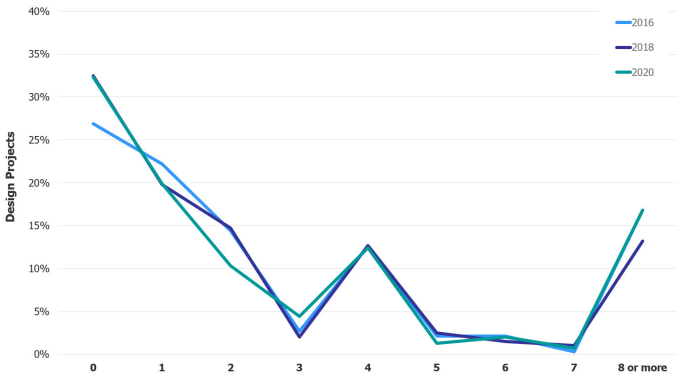

Fig. 11: Number of embedded processor cores.

B. Asynchronous clock domains

In fig. 12, we see that 88 percent of designs being implemented as IC/ASICs contain two or more asynchronous clock domains. Verifying requirements associated with multiple asynchronous clock domains has increased both the verification workload and complexity. For example, a class of metastability bugs cannot be demonstrated on an RTL model using simulation. To simulate these issues requires a gate-level model with timing, which is often not available until later stages in the design flow. Furthermore, clocking metastability bugs are generally difficult to reproduce and find in the lab. To address these issues, static clock-domain crossing (CDC) verification tools have emerged and are being adopted to help identify clock domain issues directly on an RTL model at earlier stages in the design flow.

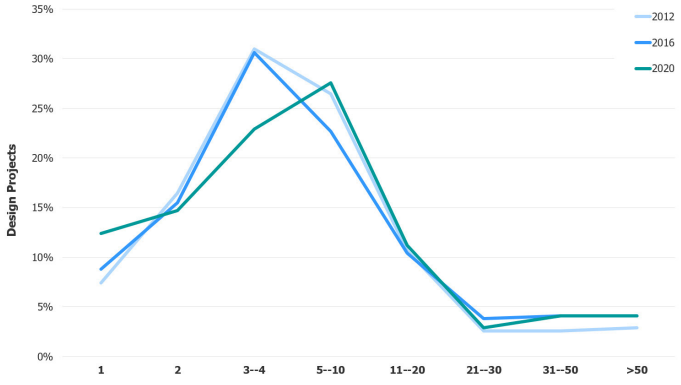

Fig. 12: Number of asynchronous clock domains.

C. Security features

Today we find that 54 percent of IC/ASIC projects add security features to their designs. Examples of security features include security assurance hardware modules (e.g., a security controller) that are designed to safely hold sensitive data, such as encryption keys, digital right management (DRM) keys, passwords, and biometrics reference data. These security features add requirements and complexity to the verification process.

D. Safety-critical design

Another example of increasing requirements contributing to complexity relates to safety-critical designs. In 2020, we find that 42 percent of all IC/ASIC projects are working under one of multiple safety-critical development process standards or guidelines. However, our 2018 study found that 59 percent of all IC/ASIC projects were working under one of multiple safety-critical development standards. We suspect the difference was due to an anomaly in the 2018 study. We know that the automotive industry is currently experiencing a contraction due to COVID-19, which might account for some of this year's decline in terms of safety critical projects. In addition, there are potentially some regional biases as discussed in the Introduction, Section D that should be considered.

For those projects working under a safety-critical development process standard or guideline, in fig. 13 we show the specific breakdown for the various standards. Note that some projects are required to work under multiple safety standards or guidelines (e.g., IEC61508 and IEC61511), which is why the percentage adoption sums to more than 100 percent.

Fig. 14 shows the percentage of overall project time spent in functional safety activities. The median percentage of time is 30 percent-40 percent. While fig. 15 shows the biggest challenges associated with functional safety as reported by this year's study participants.

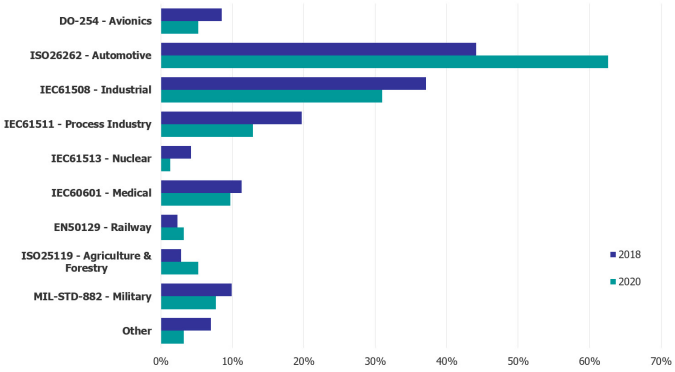

Fig. 13: Safety-critical development standard used on IC/ASIC project.

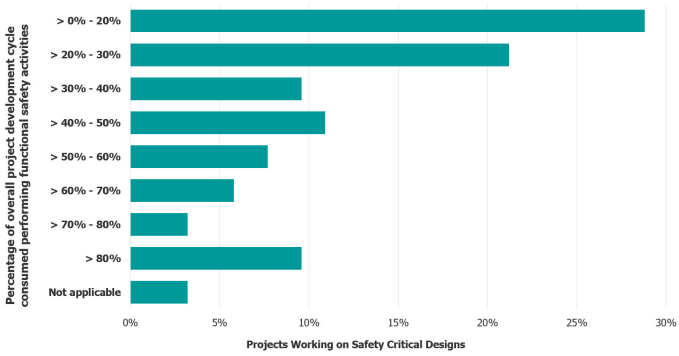

Fig. 14: Percentage of overall project time spent on functional safety.

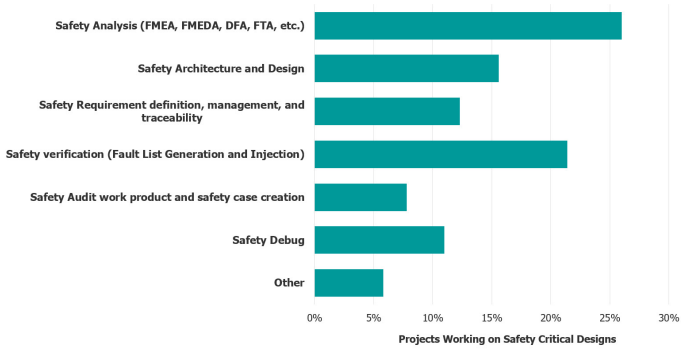

Fig. 15: Biggest functional safety project challenge.

V. IC/ASIC verification adoption trends

In this section, we present IC/ASIC trends related to the adoption of various verification techniques.

A. Verification languages and methodolgy adoption trends

In fig. 16, we show the adoption trends for languages to build testbenches. It is not uncommon for IC/ASIC projects to use multiple languages when constructing their testbenches, which is why the percentage adoption sums to more than 100 percent. This practice of adopting multiple languages is often due to legacy code as well as purchased verification IP written in a different language.

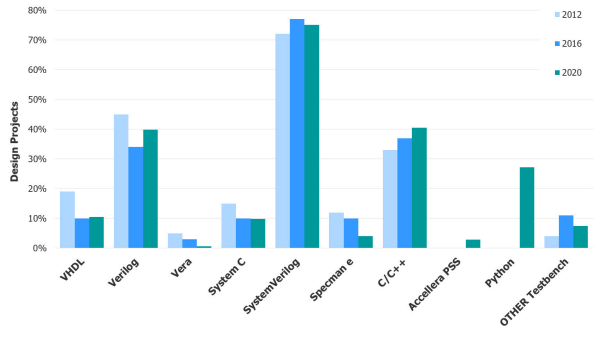

Fig. 16: IC/ASIC project verification language adoption.

In the 2020 data, we continue to see an increase in adoption of C/C++ for testbench development. In addition, we show the adoption levels for the Accellera Portable Test and Stimulus Standard (PSS). Finally, in 2020, for the first time, we explicitly asked about the adoption of Python for testbench development.

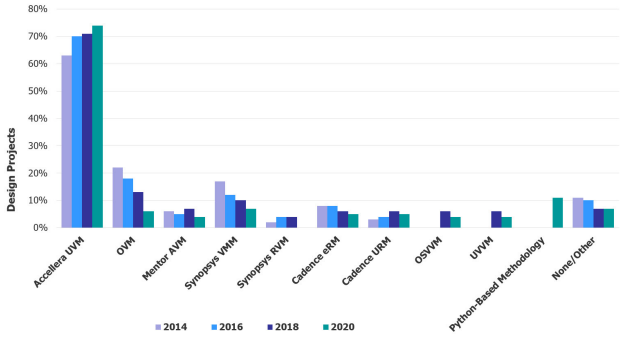

Fig. 17: IC/ASIC project methodology and base-class libraries adoption.

The adoption trends for various base-class library and methodology standards are shown in fig. 17. We found that the Accellera UVM is currently the predominant standard that has been adopted to create IC/ASIC testbenches, and it continues to grow. In 2018, we first started tracking the Open Source VHDL Verification

Methodology™ (OSVVM) and the Universal VHDL Verification Methodology (UVVM), and in 2020, we are showing trends for the first time. In addition, for the 2020 study, we are tracking Python-based methodologies, such as cocotb, for the first time.

Finally, IC/ASIC project adoption trends for various assertion language standards are shown in fig. 18. SystemVerilog Assertions (SVA) is the predominant assertion language in use today. Similar to languages used to build testbenches, it is not unusual to find IC/ASIC projects create their RTL in VHDL and then create their assertions using SVA.

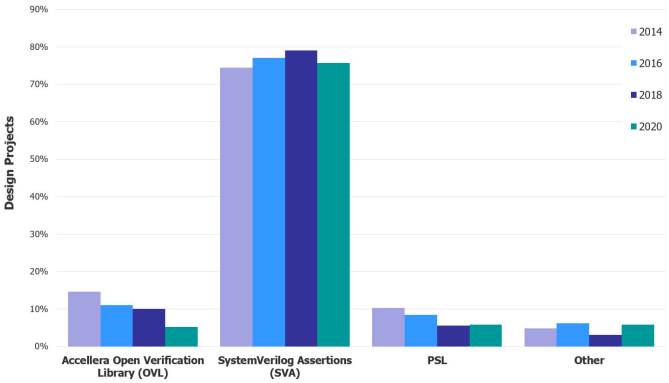

Fig. 18: IC/ASIC project assertion lanauge adption.

B. Verification technology adoption trends

The adoption trends for formal property checking (e.g., model checking) and automatic formal applications are shown in fig. 19. We found that the adoption of formal property checking on IC/ASIC projects is growing at a 6.7 percent CAGR, and the adoption of automatic formal applications is growing at an impressive 13.2 percent CAGR.

Historically, the formal property checking process has required specialized skills and expertise. However, the recent emergence of automatic formal applications provides narrowly focused solutions and does not require specialized skills for adoption. In general, formal solutions (i.e., formal property checking combined with automatic formal applications) is one of the fastest growing segments in functional verification in terms of project adoption.

Fig. 20 shows the IC/ASIC project adoption trends for various simulation-based techniques from 2012 through 2018, which include code coverage, functional coverage, assertions, and constrained-random simulation. One observation from these adoption trends is that the IC/ASIC market continues to mature its verification processes.

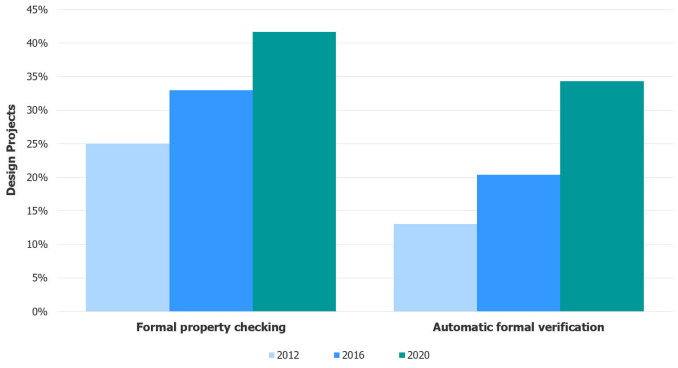

Fig. 19: IC/ASIC project formal technology adoption trends.

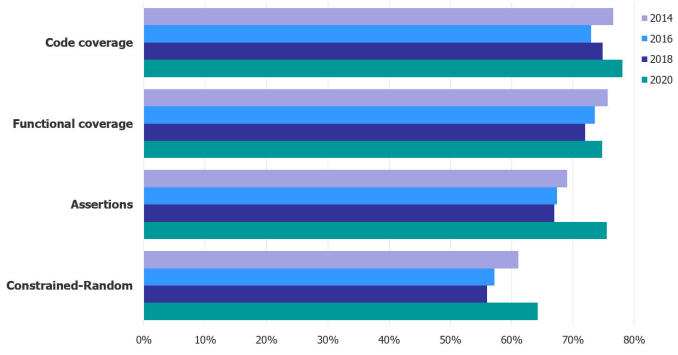

Fig. 20: IC/ASIC project simulation technique trends.

VI. Emulation and FPGA prototyping

Historically, the simulation market has depended on processor frequency scaling as one means of continual improvement in simulation performance. However, as processor frequency scaling levels off, simulation-based techniques are unable to keep up with today's growing complexity. This is particularly true when simulating large designs that include both software and embedded processor core models. Hence, acceleration techniques are now required to extend verification performance for many designs. In fact, emulation and FPGA prototyping have become key platforms for SoC integration verification where both hardware and software are integrated into a system for the first time. In addition to SoC verification, emulation and FPGA prototyping are also used today as a platform for software development. Fig. 21 describes various reasons why projects are using these techniques. You might note that the results do not sum to 100 percent since multiple answers were accepted from each study participant.

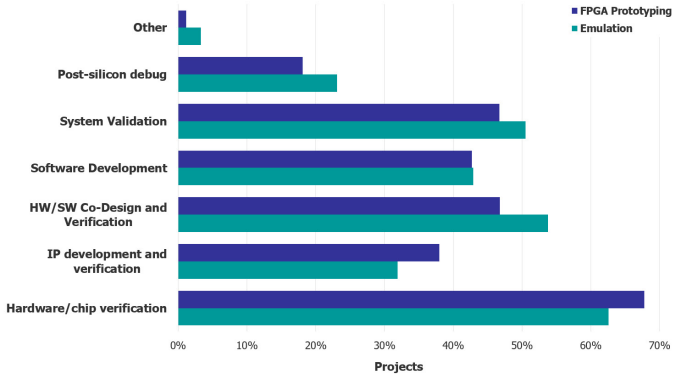

Fig. 21: Why was emulation or FPGA prototyping used?

Fig. 22 partitions the data for emulation and FPGA prototyping adoption by the design size as follows: less than 1M gates, 1M to 80M gates, and greater than 80M gates. Notice that the adoption of emulation continues to increase as design sizes increase. However, the adoption of FPGA prototyping does not follow a similar trend as design sizes increase beyond 80M gates.

This graph illustrates one of the problems with adopting FPGA prototyping of very large designs. That is, an increased engineering effort required to partition designs across multiple FPGAs. In fact, the FPGA prototyping of very large designs is often a major engineering effort in itself, and one that many projects are trying to find alternative solutions for (e.g., virtual prototyping or actual silicon as a validation platform). Nonetheless, FPGA prototyping is still a critical process required for many of today's large, complex designs.

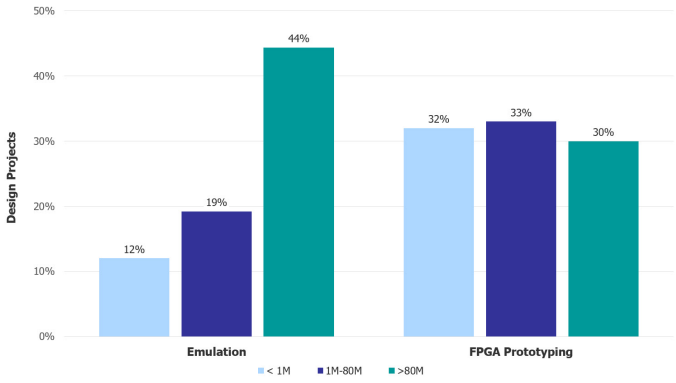

Fig. 22: Emulation and FPGA Prototyping adoption by design size.

VII. Conclusion

This report presents the findings from a recent worldwide, double-blind, functional verification study, covering all electronic industry market segments. This study quantitatively provides insight into today's functional verification process in terms of verification technology adoption, effort, and effectiveness.

The data our study reveals is certainly of value, but it does not represent all challenges associated with SoC design (such as system validation). In fact, many of the techniques used for block and subsystem verification that we studied do not scale well to the full SoC integration and system-level validation space (e.g., constrained-random, functional coverage, and general formal property checking). In addition, our study does not encompass analog, mixed-signal, ESL, nor virtual prototyping. We believe that future studies should be expanded to include these emerging challenges.

Finally, it is our belief that the benefit from this year's industry study is not necessarily the quantitative values that the findings reveal but the new questions they raise and the healthy dialogue that ensues.

Acknowledgment

The author would like to thank Zachary Wilson (from Wilson Research Group), in addition to Merlyn Brunken and Susan Hanson (from Siemens Digital Industries Software) for their expertise and guidance in conducting very large industry studies.

References

1. R. Collett, "2002 IC/ASIC functional verification study," Industry Report from Collett International Research, Inc., 2003.
2. R. Collett, "2004 IC/ASIC functional verification study," Industry Report from Collett International Research, Inc., 2005.
3. H. Foster, "Why the design productivity gap never happened" in Proceedings of the International Conference on Computer-Aided Design (ICCAD), IEEE Press pp. 581-584, San Jose, California, Nov. 2013
4. H. Foster, "Trends in functional verification: a 2014 industry study," Proceedings of the 52nd Annual Design Automation Conference (DAC), p.1-6, San Francisco, California, Jun. 2015.
5. H. Foster, "Trends in functional verification: a 2016 industry study," DVCon 2017, San Jose, California, Mar. 2017.
6. H. Foster, "2018 FPGA Functional Verification Trends," in 19th International Workshop on Microprocessor and SOC Test and Verification (MTV), Austin, TX, USA, Dec. 2018.
7. IC-Insights, April Update to The McCLEAN REPORT 2020 EDITION, April, 2020.
8. International Business Strategies, Semiconductor Market Analysis, Volume 29, No. 1, January, 2020.
9. W. Chen, Member, S. Ray, M. Abadir, J. Bhadra, Li-C Wang, Challenges and Trends in Modern SoC Design Verification, IEEE Design & Test,Vol 34, Issue: 5, Oct. 2017

Siemens Digital Industries Software

Headquarters
Granite Park One
5800 Granite Parkway
Suite 600
Plano, TX 75024
USA
+1 972 987 3000

Americas
Granite Park One
5800 Granite Parkway
Suite 600
Plano, TX 75024
USA
+1 314 264 8499

Europe
Stephenson House
Sir William Siemens Square
Frimley, Camberley
Surrey, GU16 8QD
+44 (0) 1276 413200

Asia-Pacific
Unit 901-902, 9/F
Tower B, Manulife Financial Centre
223-231 Wai Yip Street, Kwun Tong
Kowloon, Hong Kong
+852 2230 3333

About Siemens Digital Industries Software

Siemens Digital Industries Software is driving transformation to enable a digital enterprise where engineering, manufacturing and electronics design meet tomorrow. Xcelerator, the comprehensive and integrated portfolio of software and services from Siemens Digital Industries Software, helps companies of all sizes create and leverage a comprehensive digital twin that provides organizations with new insights, opportunities and levels of automation to drive innovation. For more information on Siemens Digital Industries Software products and services, visit siemens.com/software or follow us on LinkedIn, Twitter, Facebook and Instagram. Siemens Digital Industries Software – Where today meets tomorrow.

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