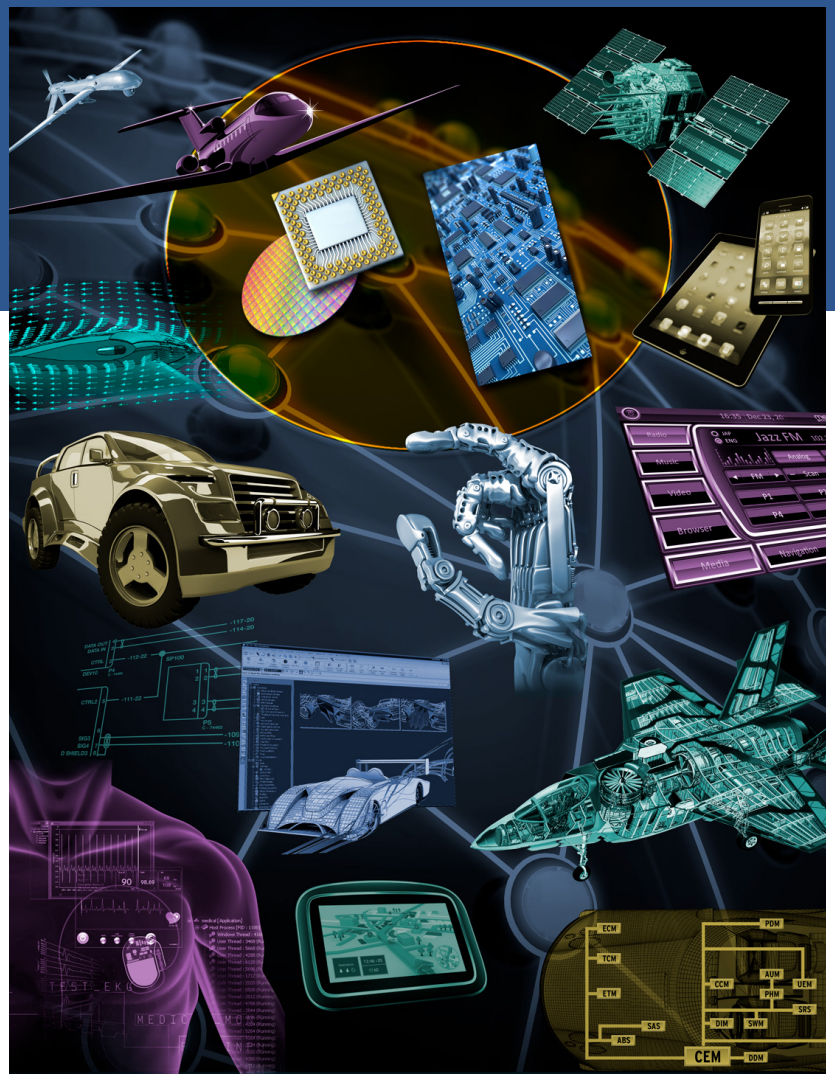


2020 Wilson Research Group Functional Verification Study

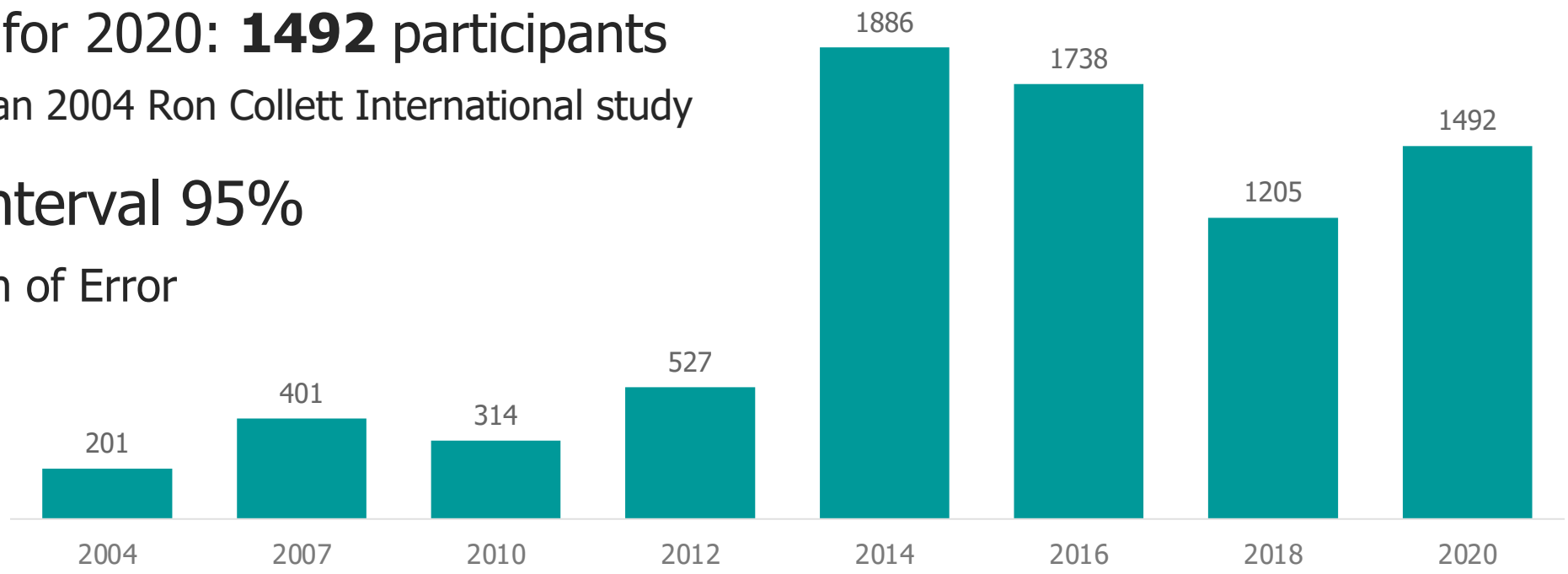
Harry Foster

October 2020

Mentor®
A Siemens Business

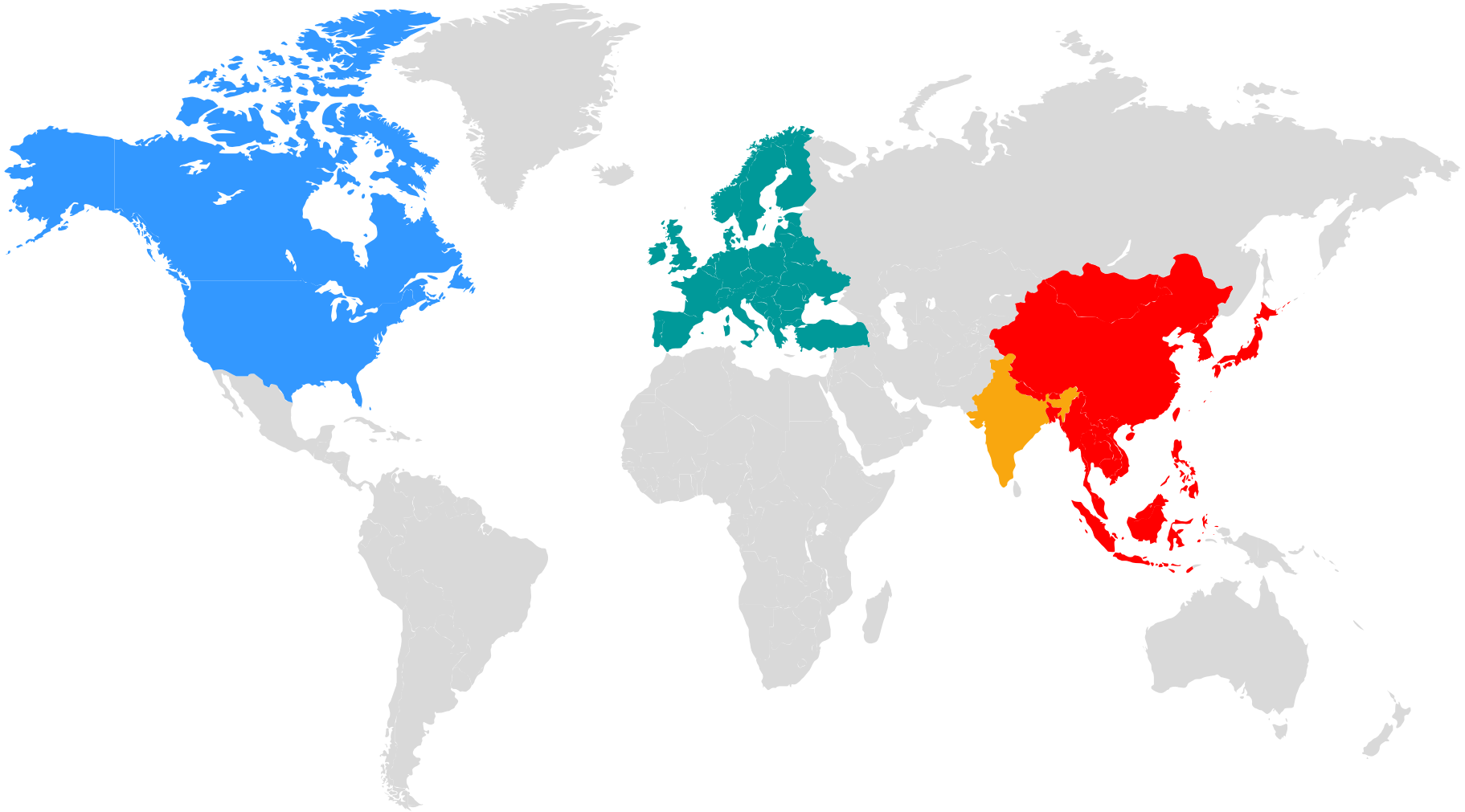
2020 Study Background

- Our worldwide study is highly respected and referenced
  - Study pool not based on Mentor's customer list
  - Double blind study
- Sample frame for 2020: **1492** participants
  - **7.4x** larger than 2004 Ron Collett International study
- Confidence interval 95%
  - **±3%** Margin of Error



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

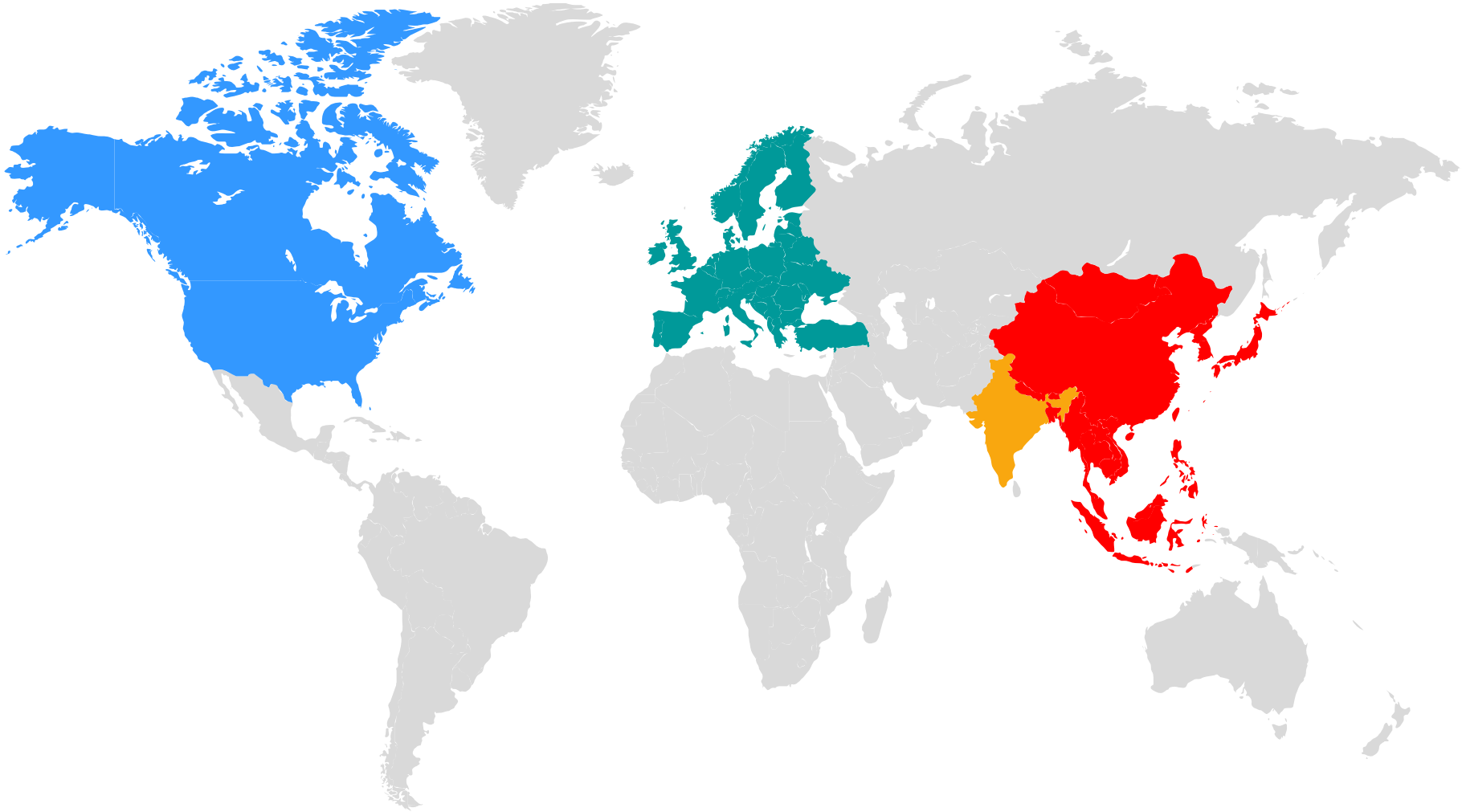
2020 Study Demographics

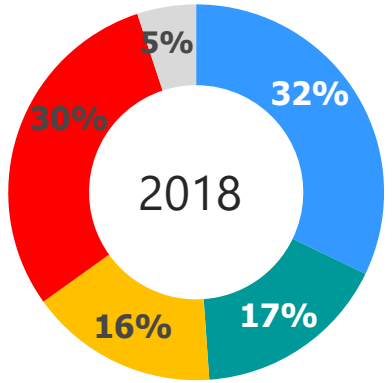


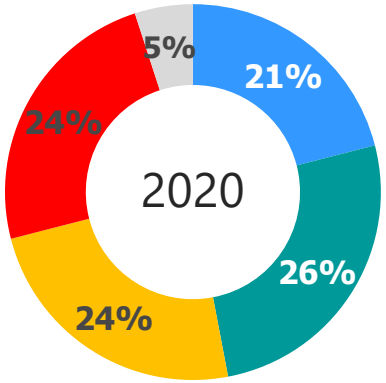
21%	North America
26%	Europe
24%	India
24%	East Asia
5%	Other

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

2018 vs 2020 Study Demographics







Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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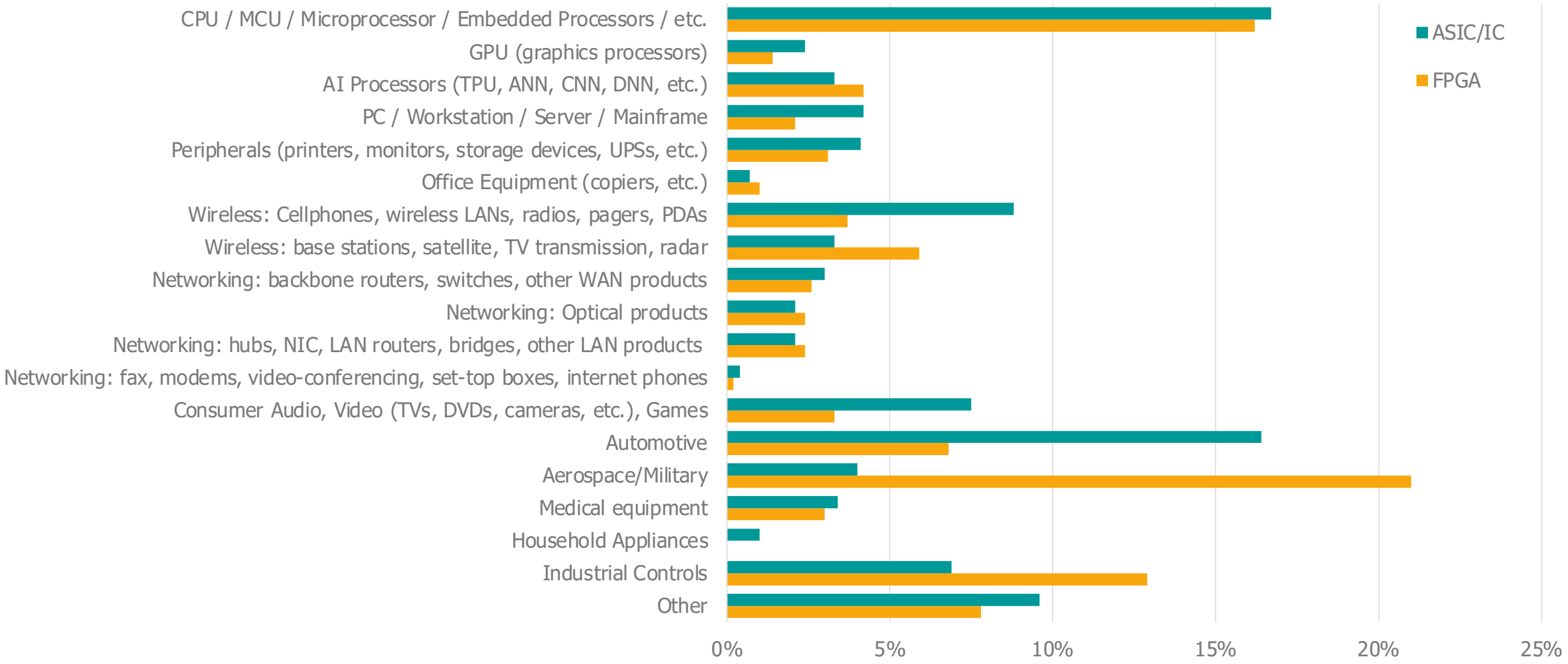
2020 Study Participation by Market Segment



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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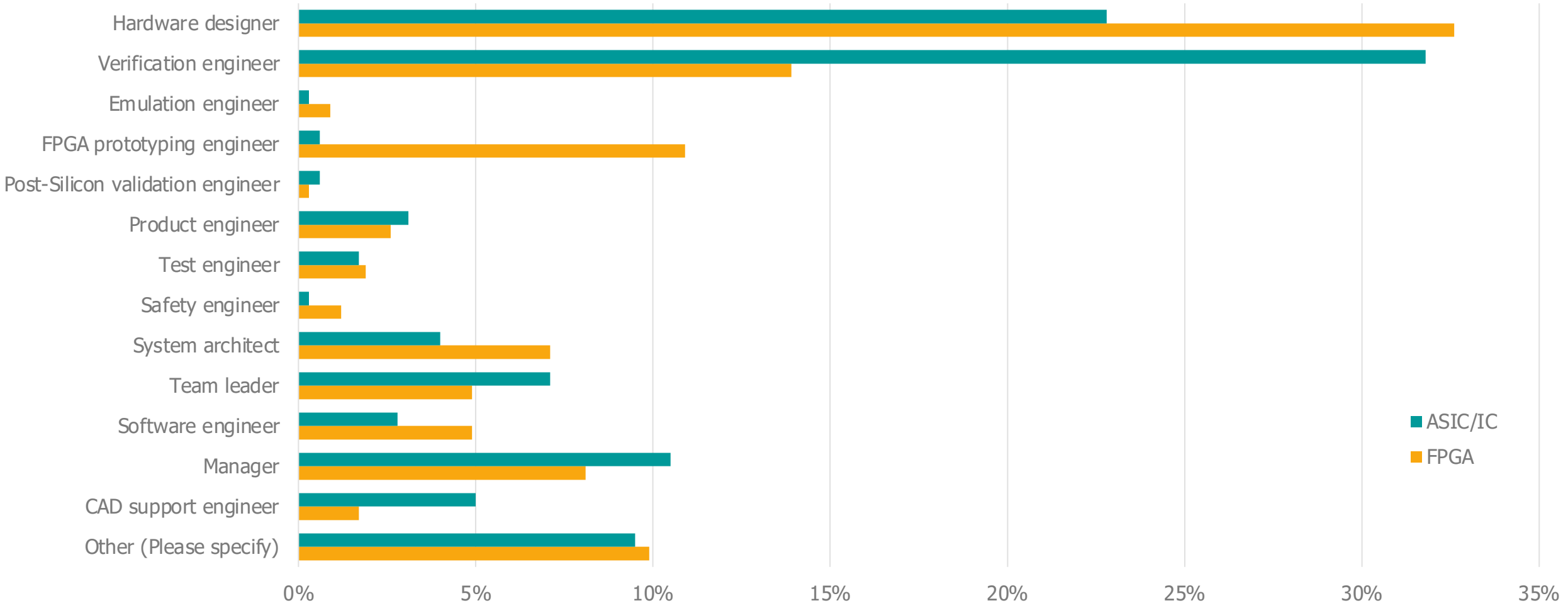
2020 Study Participation by Job Title



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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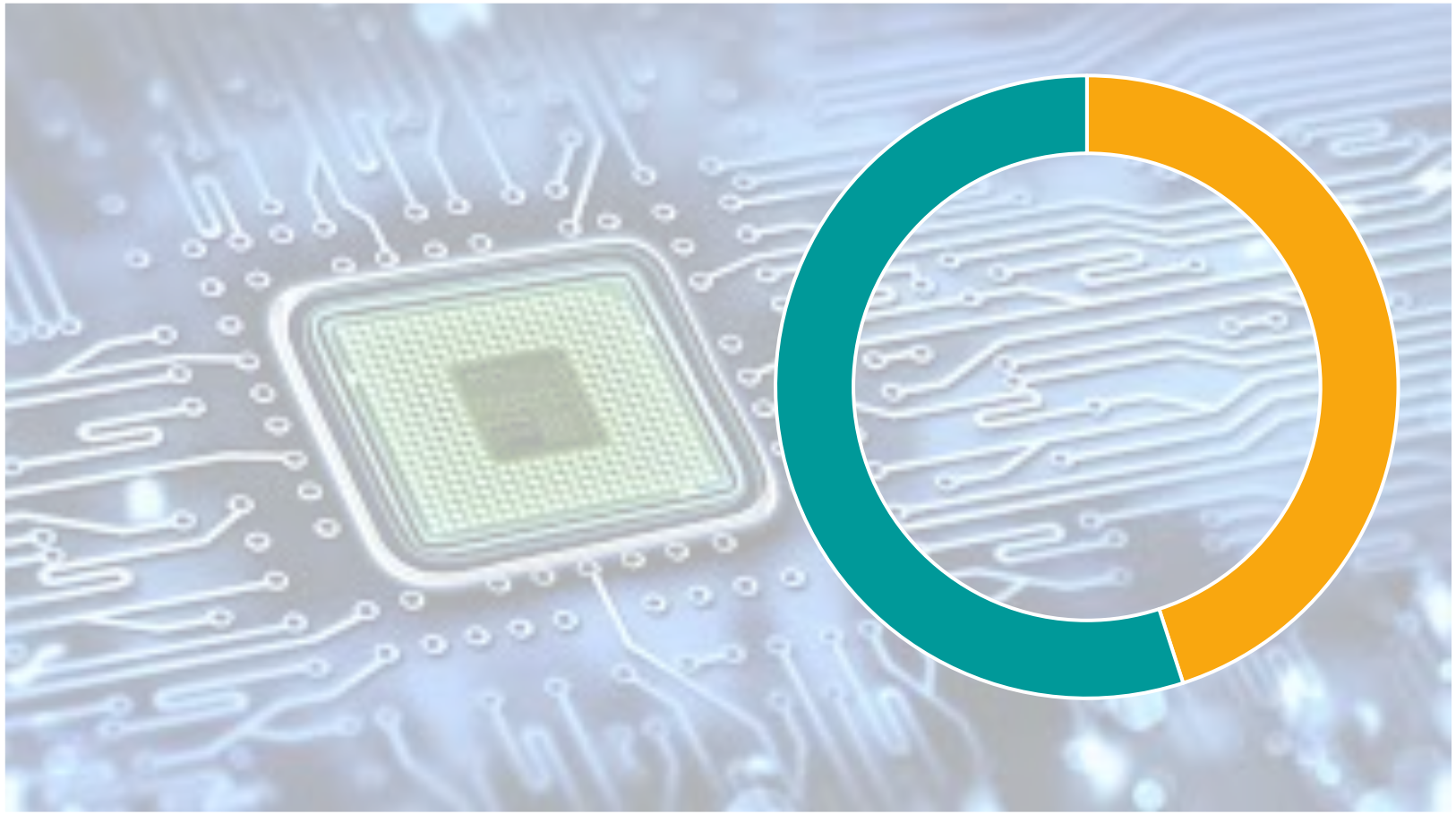
PARTICIPANT’S CURRENT DESIGN

2020 Study Participation by Targeted Implementation

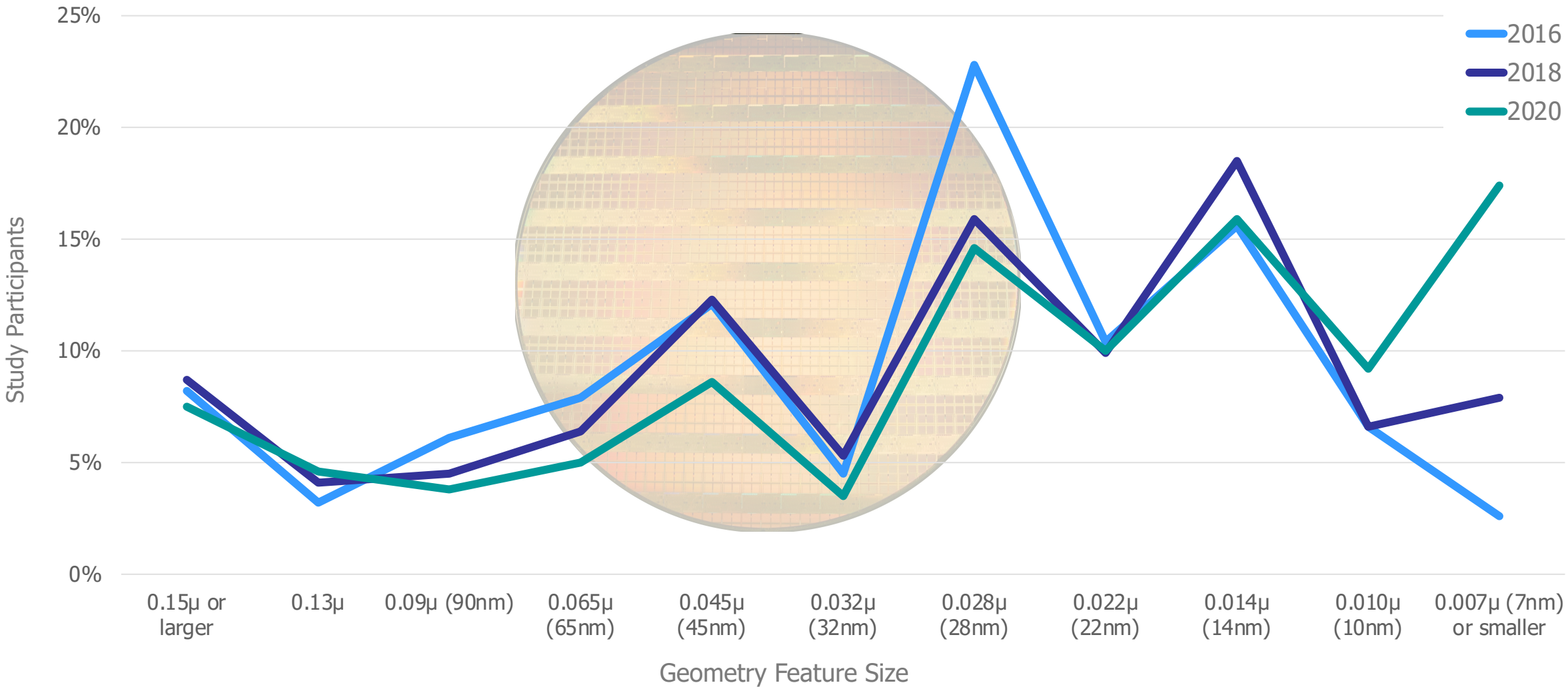


55% ASIC/IC

45% FPGA

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

Study Participation by Geometry Feature Size



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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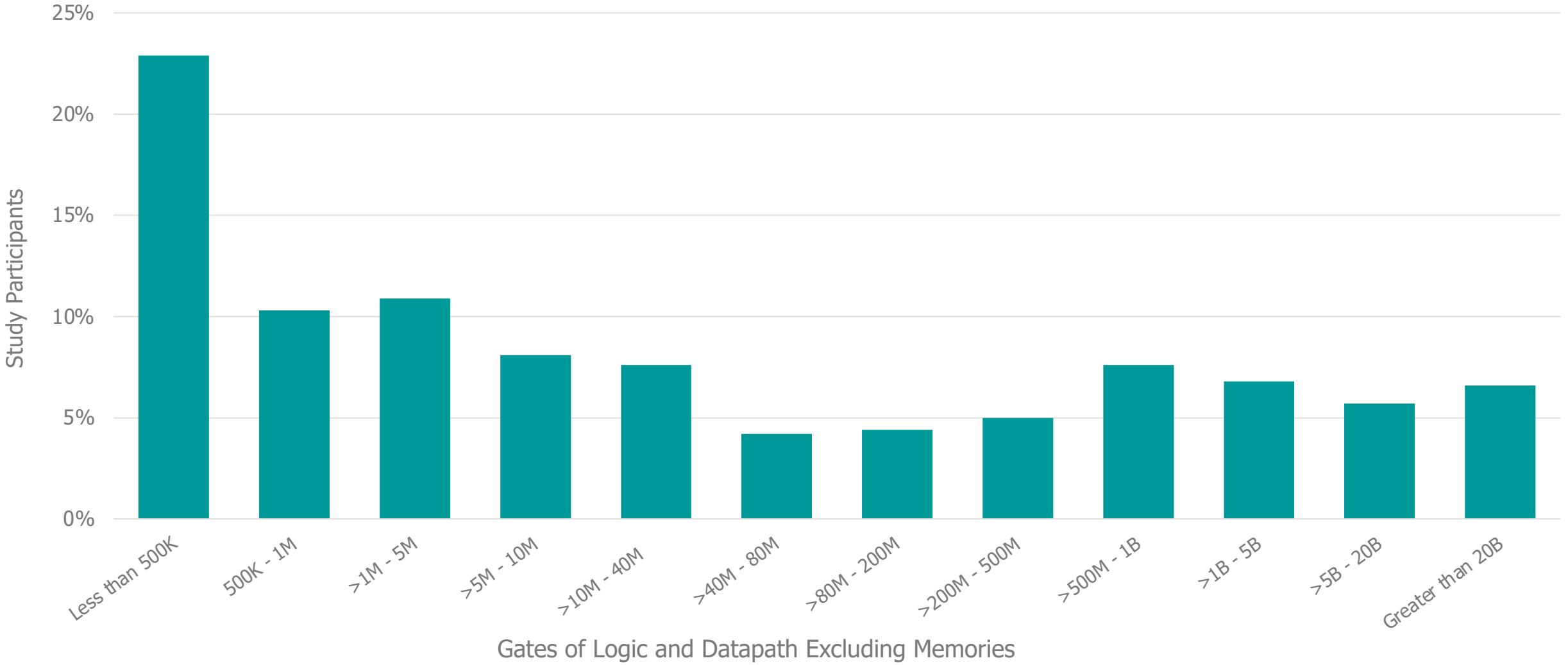
2020 ASIC Study Participation by Gate Count



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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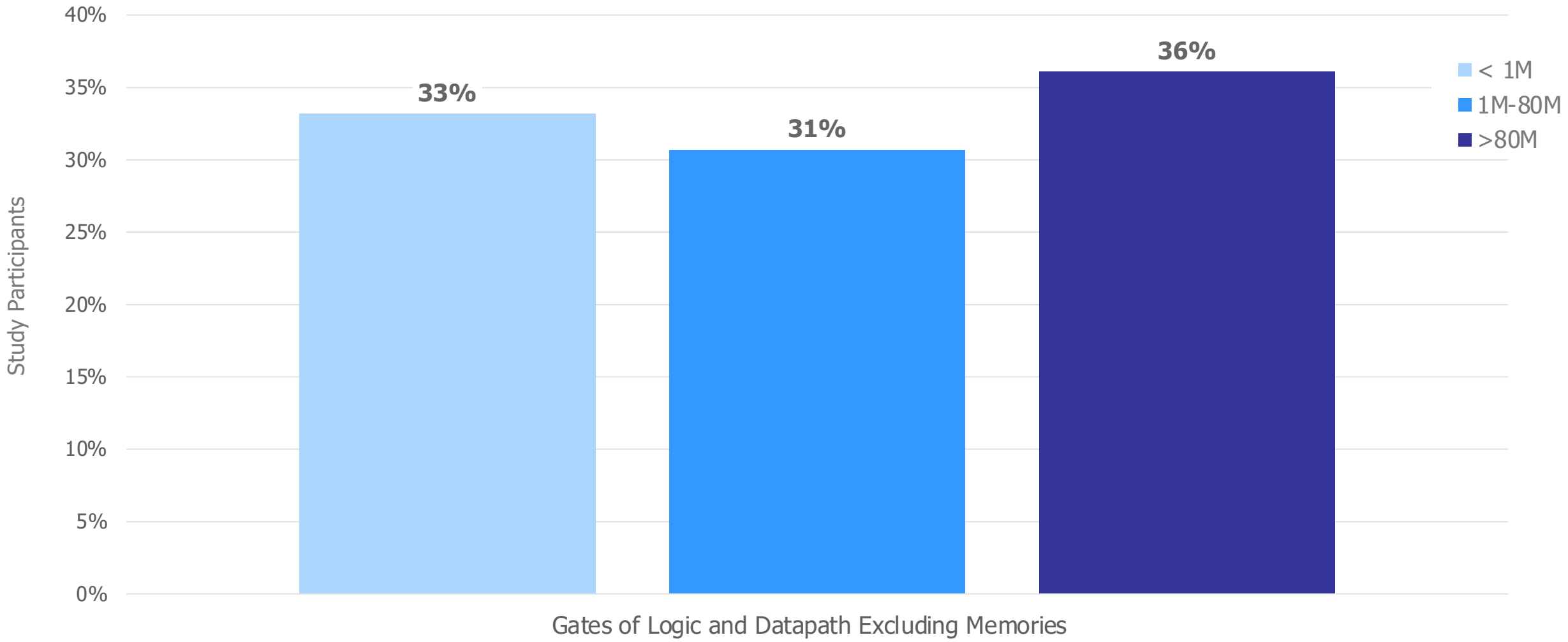
2020 ASIC Study Participants by Design Size



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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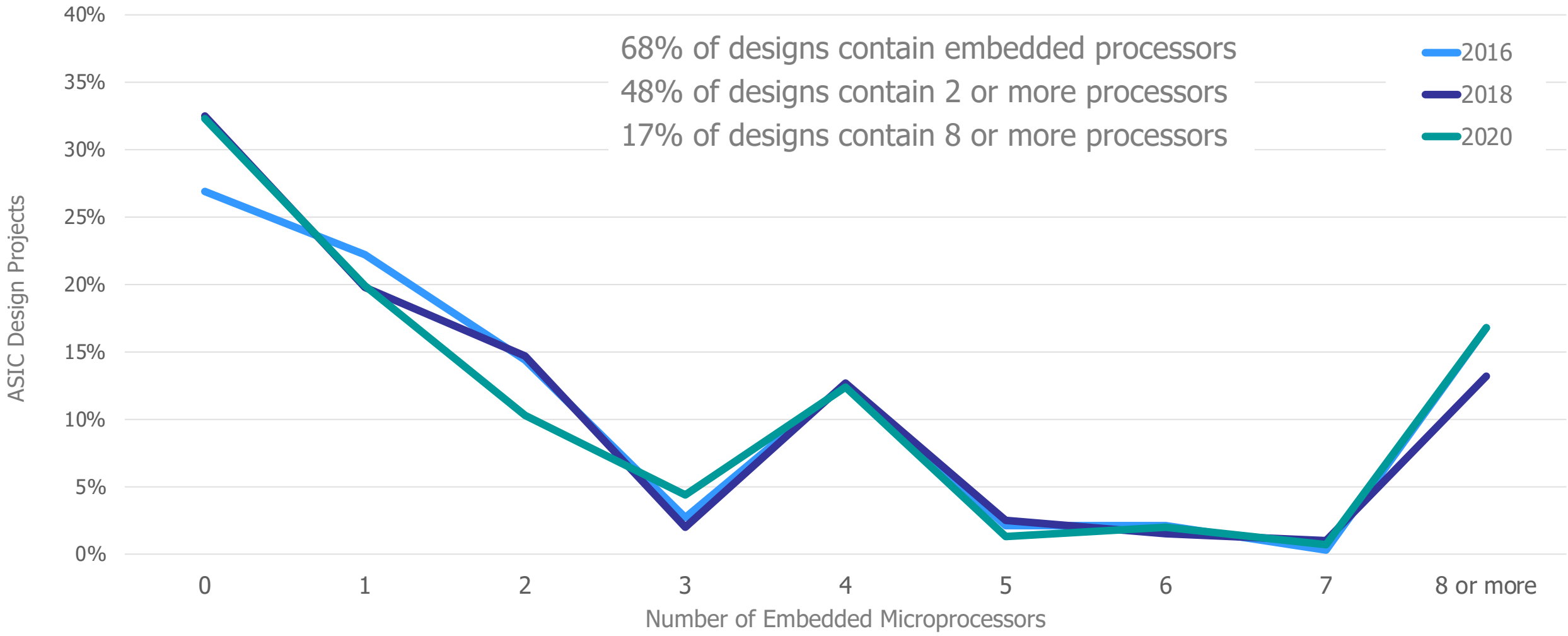
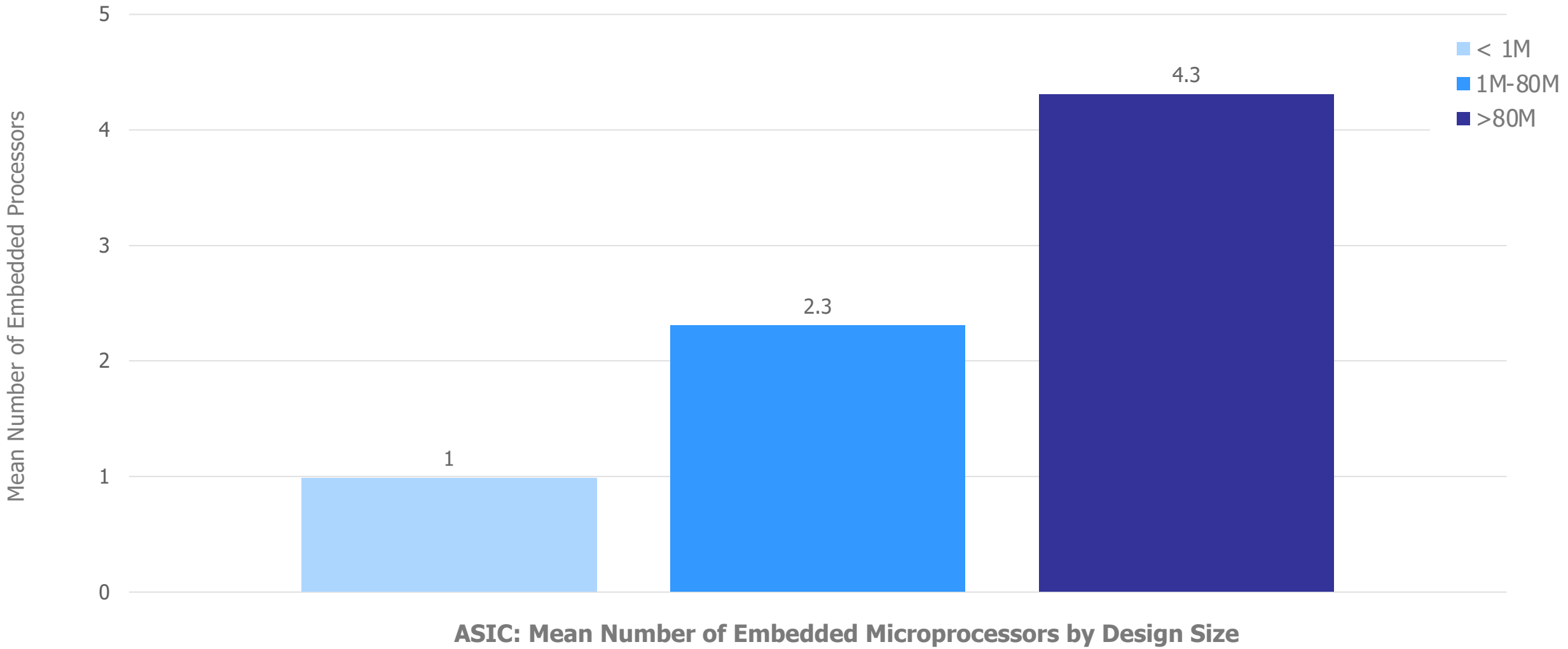
ASIC Number of Embedded Microprocessors



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

ASIC Mean Number of Embedded Microprocessors by Design Size



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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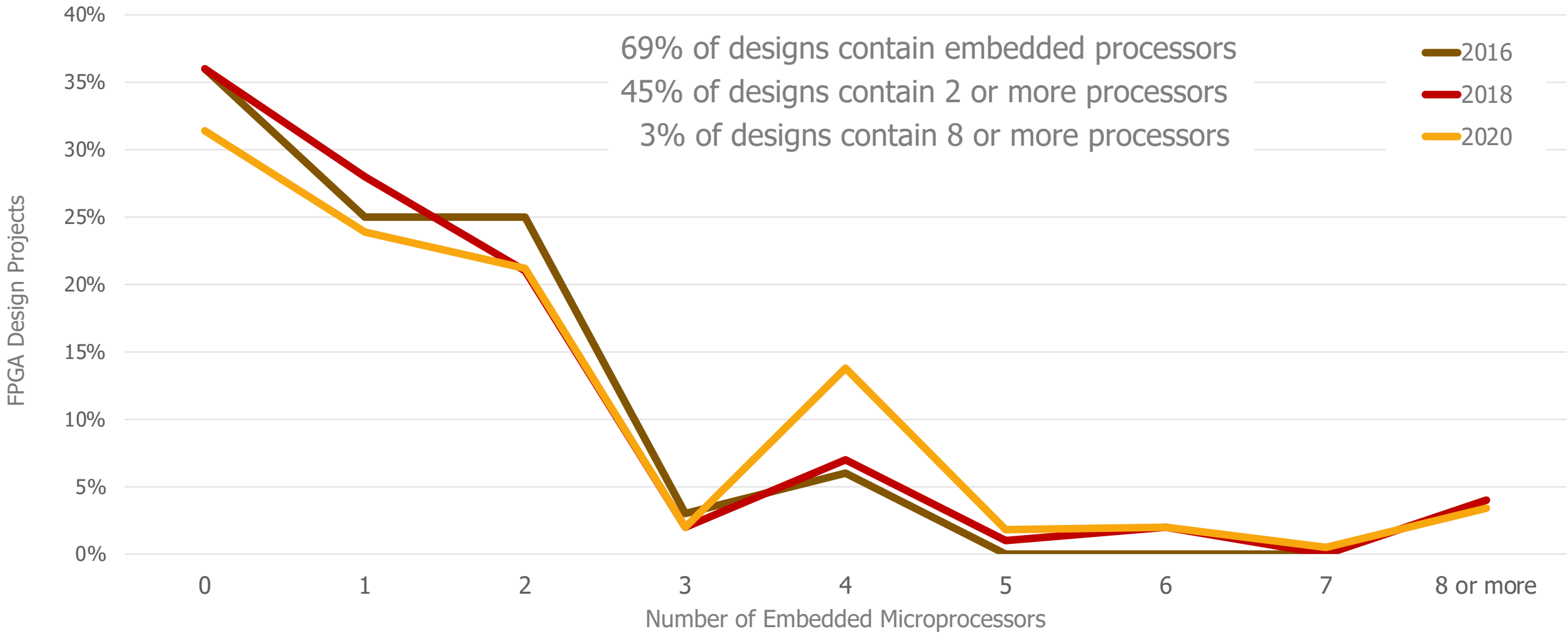
FPGA Number of Embedded Microprocessors



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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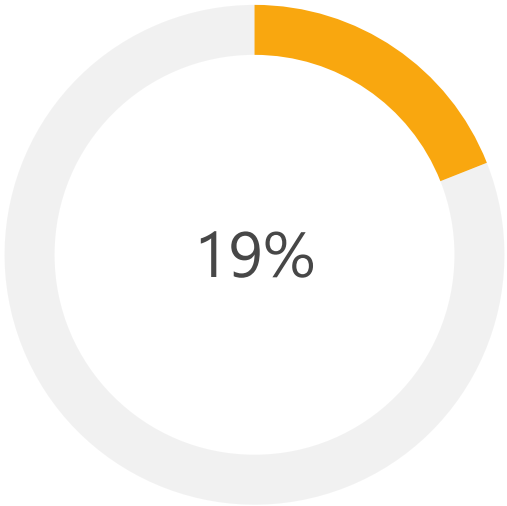
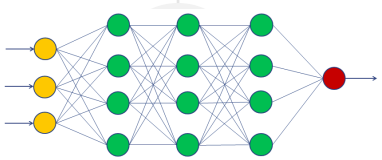
Projects Incorporating AI Processors/Accelerators

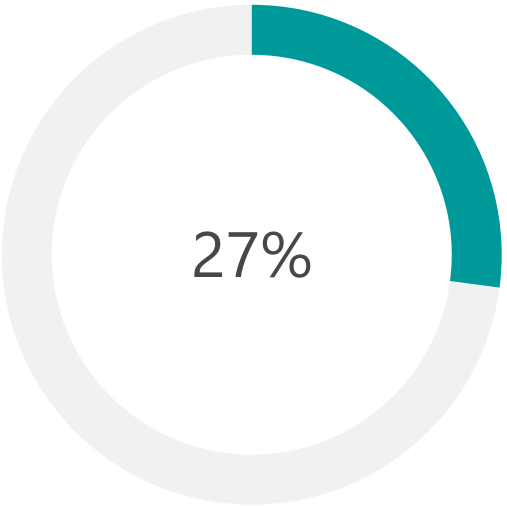
FPGA



Percentage of FPGA designs that contain any artificial intelligence processors or accelerators?



ASIC/IC

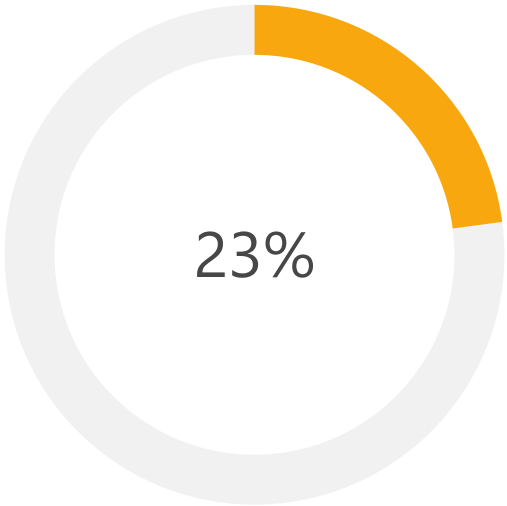


Percentage of ASIC/IC designs that contain any artificial intelligence processors or accelerators?

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

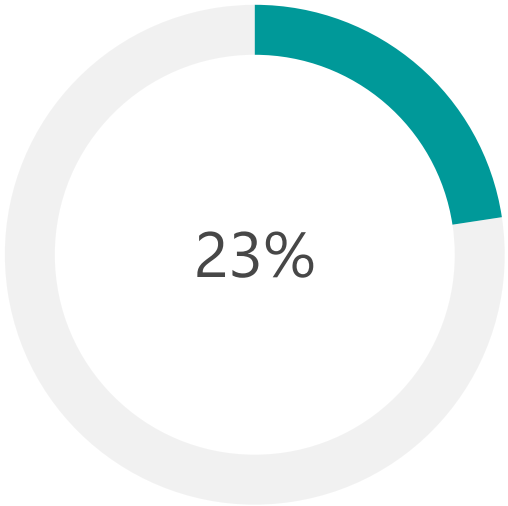
Projects Incorporating RISC-V Processors in Design

FPGA



Percentage of FPGA designs that contain a RISC-V processor in the design.

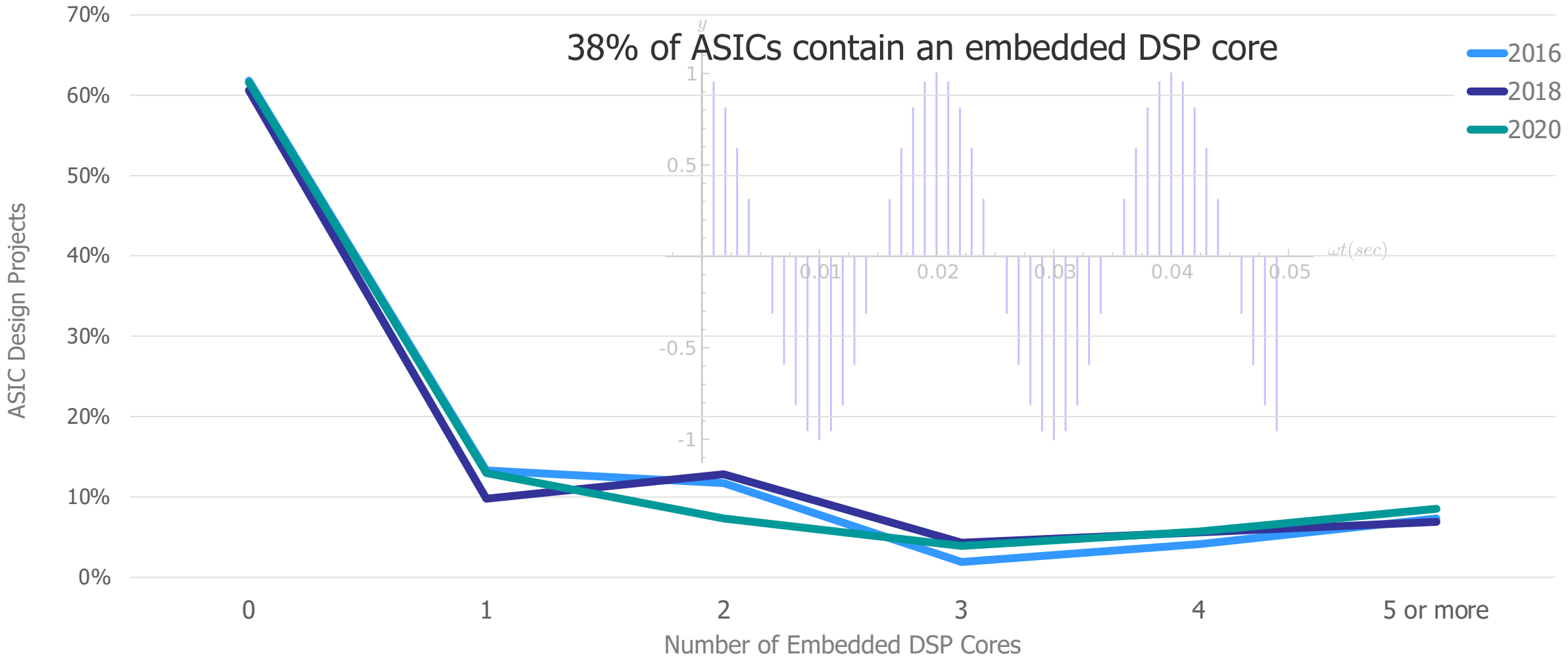
ASIC/IC



Percentage of ASIC/IC designs that contain a RISC-V processor in the design.

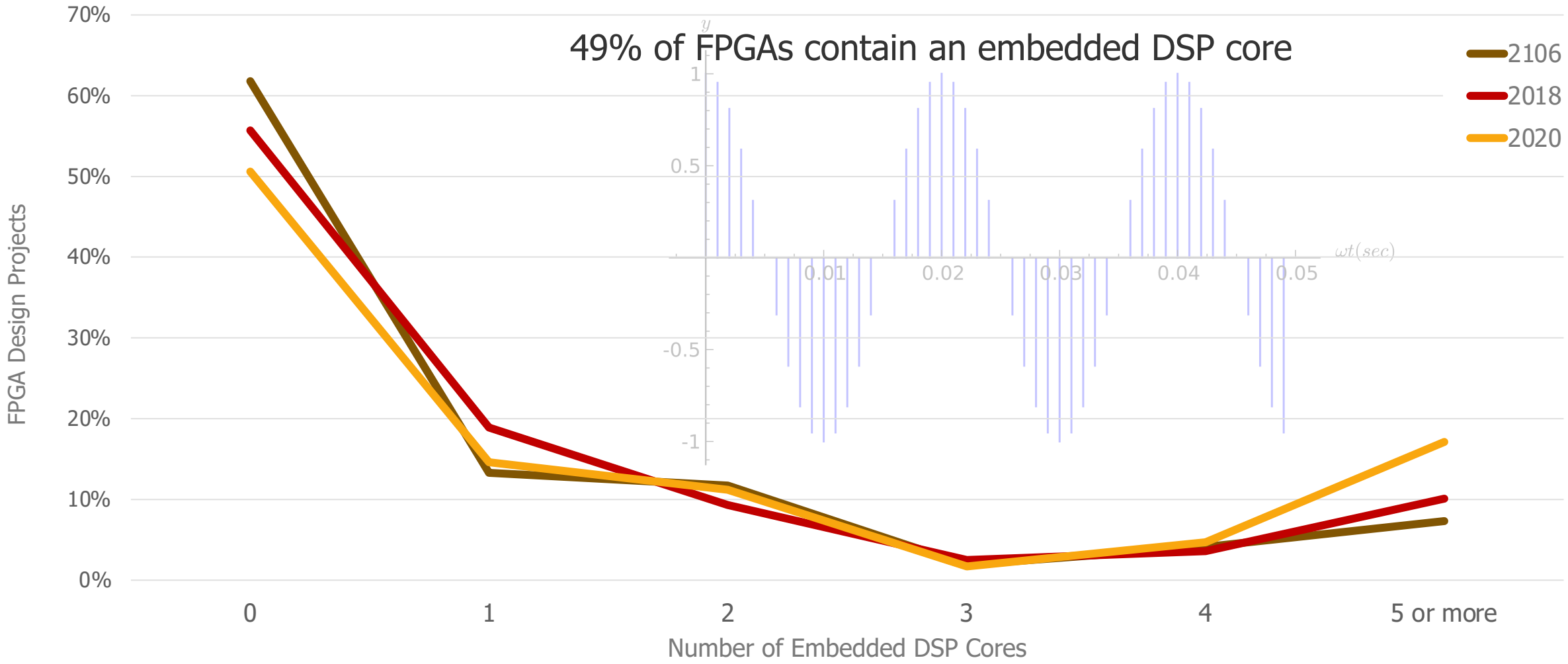
Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

ASIC Number of Embedded DSP Cores



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

FPGA Number of Embedded DSP Cores



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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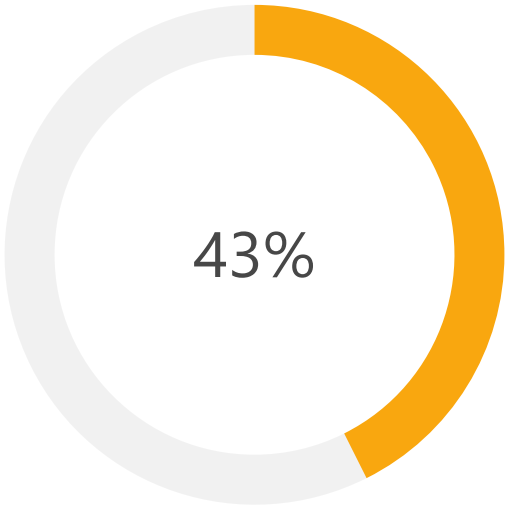
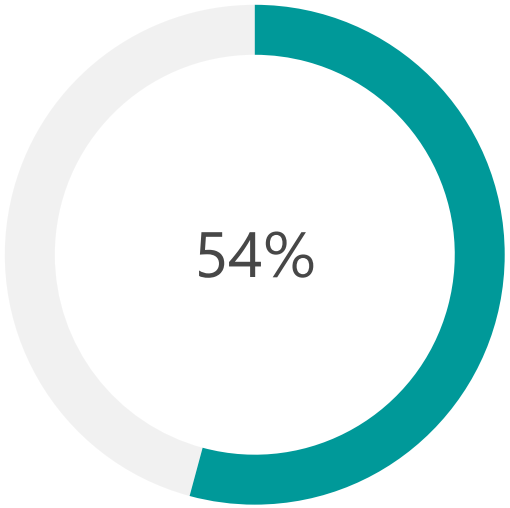
Design Projects Implementing Security Features

FPGA



Percentage of FPGA projects implementing hardware security features in your design that you must verify.

ASIC/IC

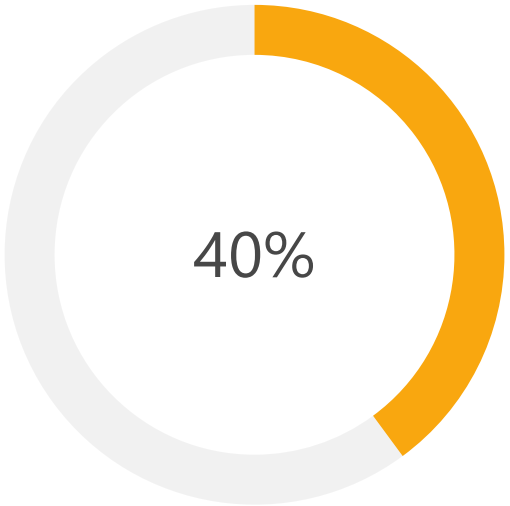


Percentage of ASIC/IC projects implementing hardware security features in your design that you must verify.

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

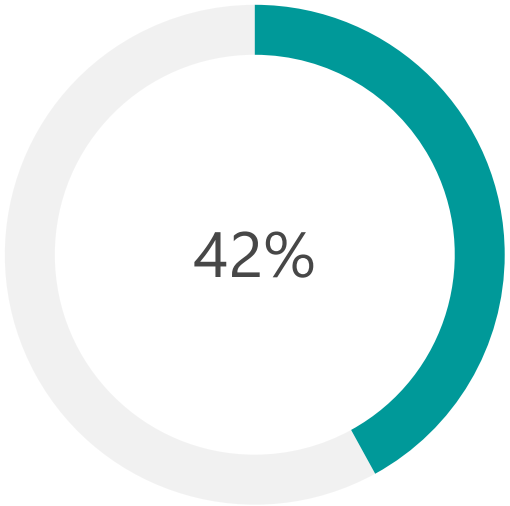
Projects Working on Safety Critical Design

FPGA



Percentage of FPGA projects working on a safety critical development standard (e.g., DO-254, ISO26262, IEC60601, IEC61508, etc.)

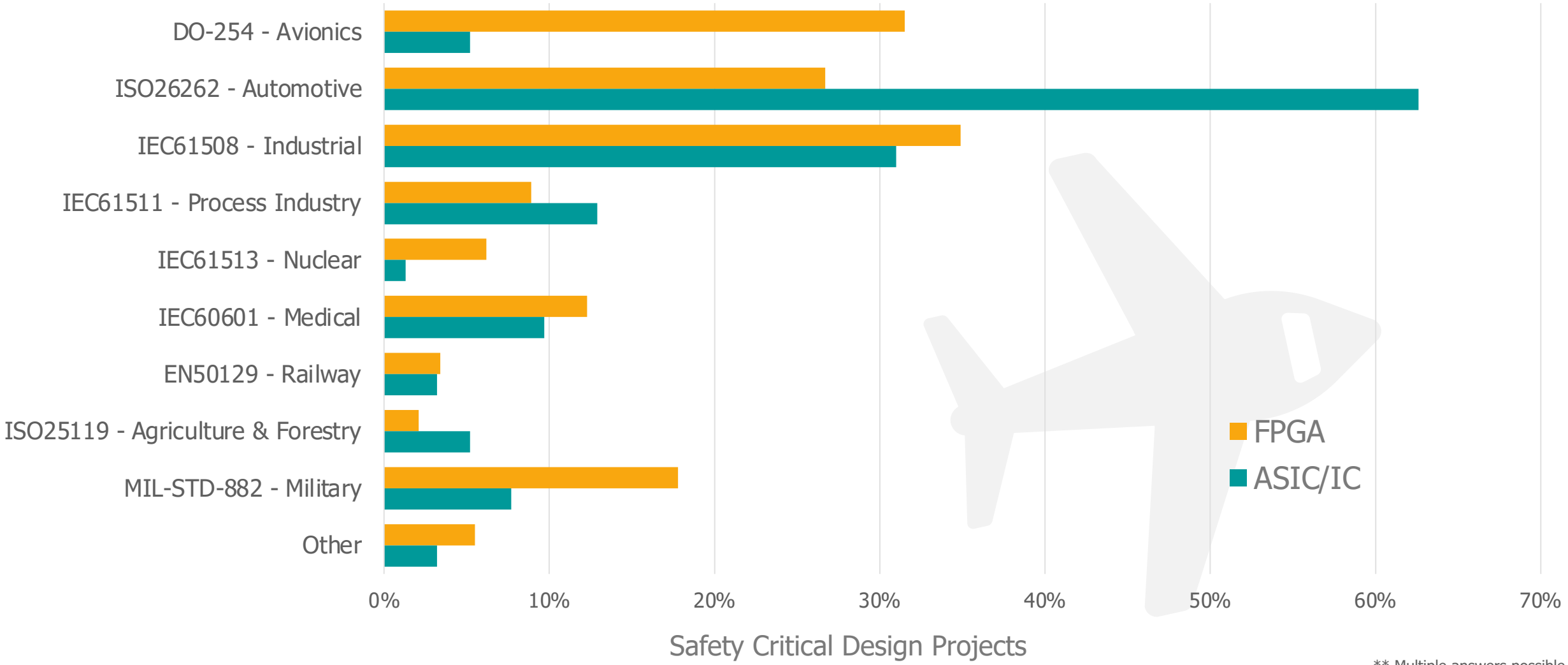
ASIC/IC



Percentage of ASIC/IC projects working on a safety critical development standard (e.g., DO-254, ISO26262, IEC60601, IEC61508, etc.)

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

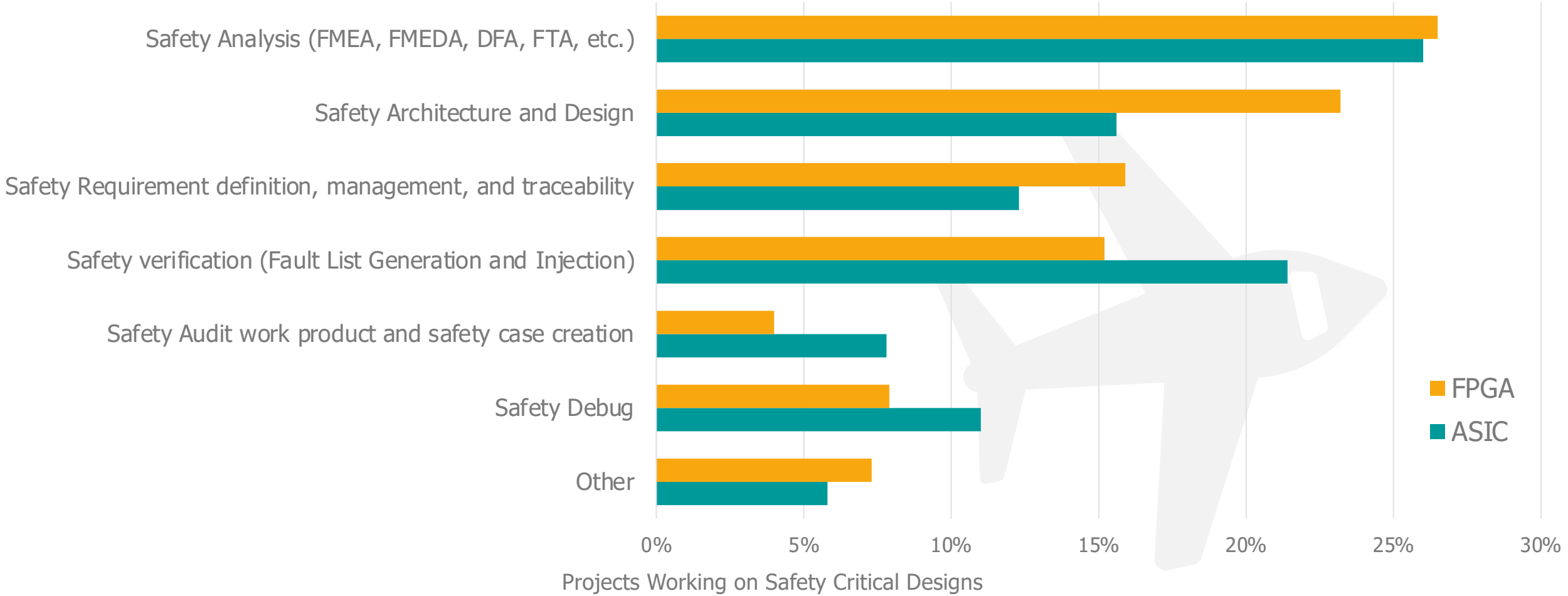
Adoption of Various Functional Safety Standards



** Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

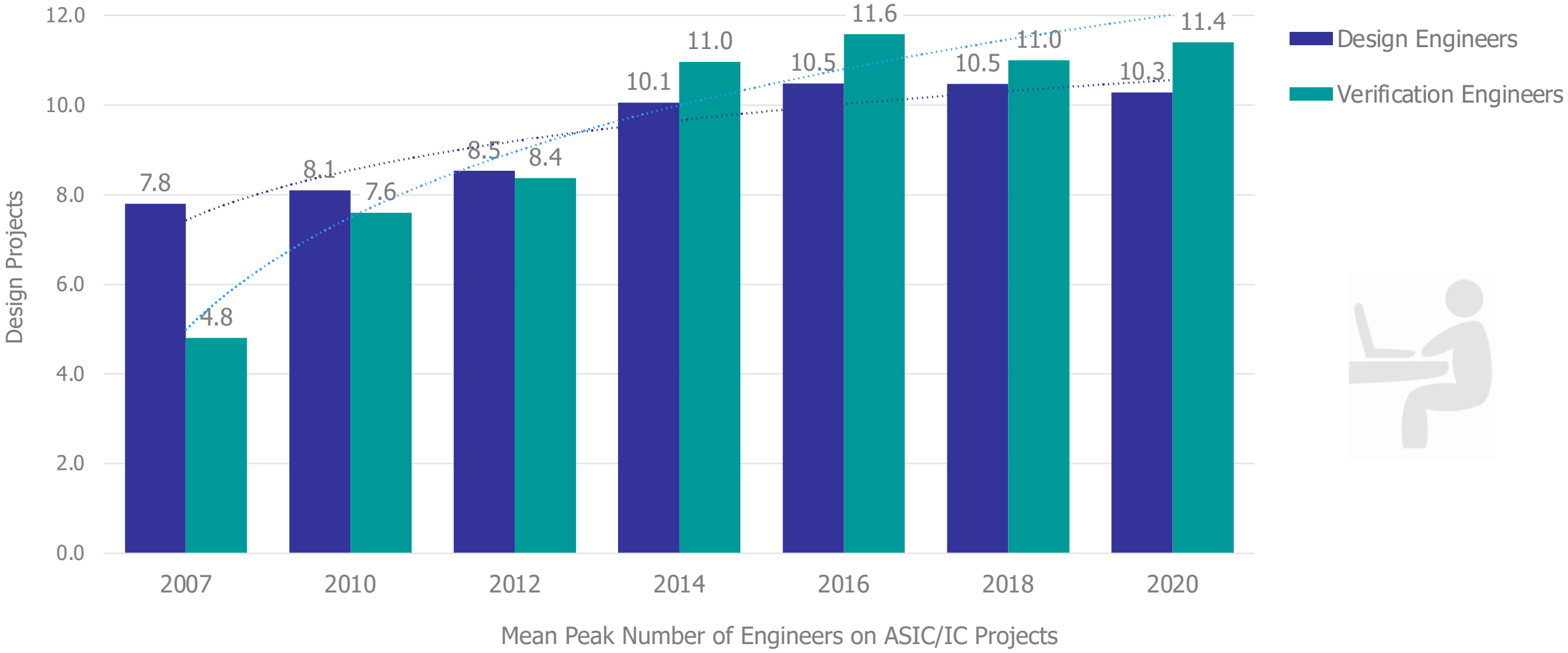
Biggest Functional Safety Project Challenge



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

PROJECT RESOURCES

Mean Peak Number of Engineers on an ASIC/IC Project



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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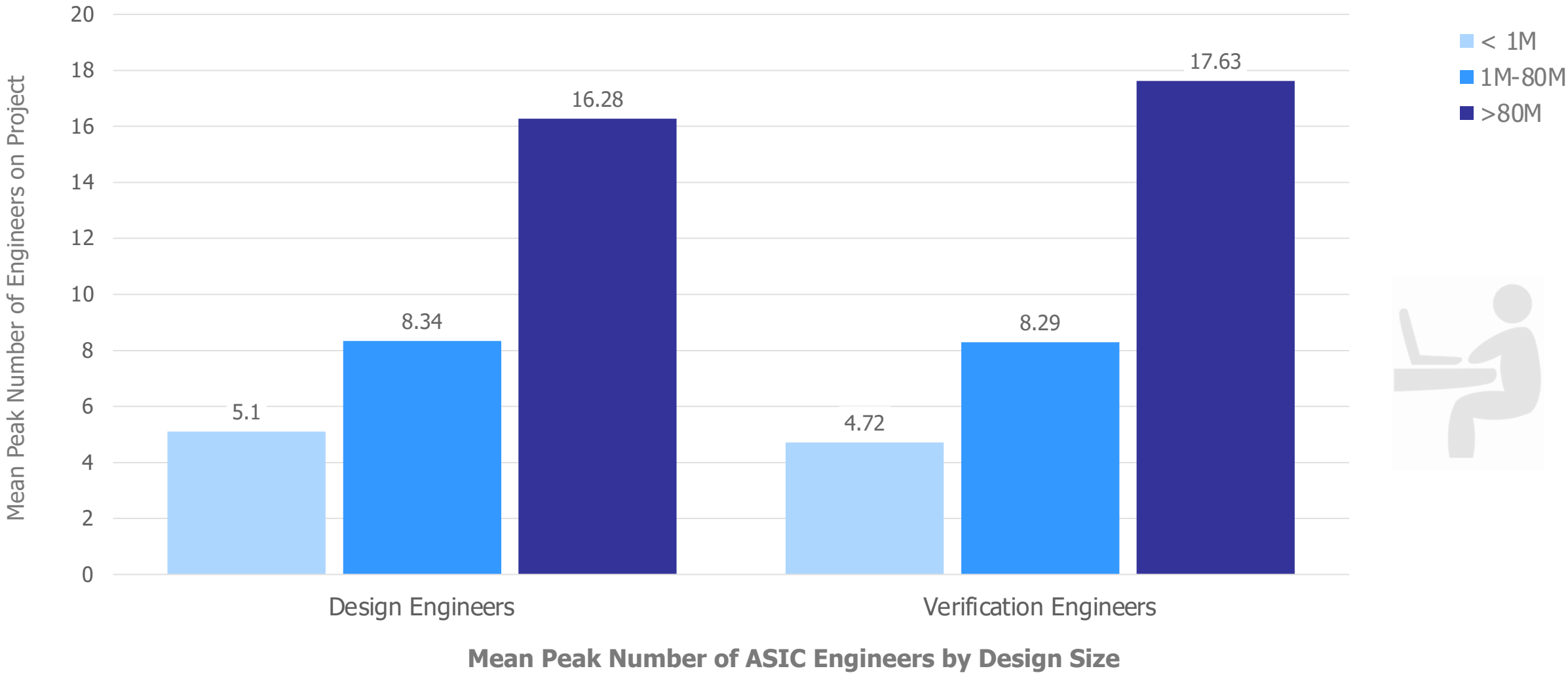
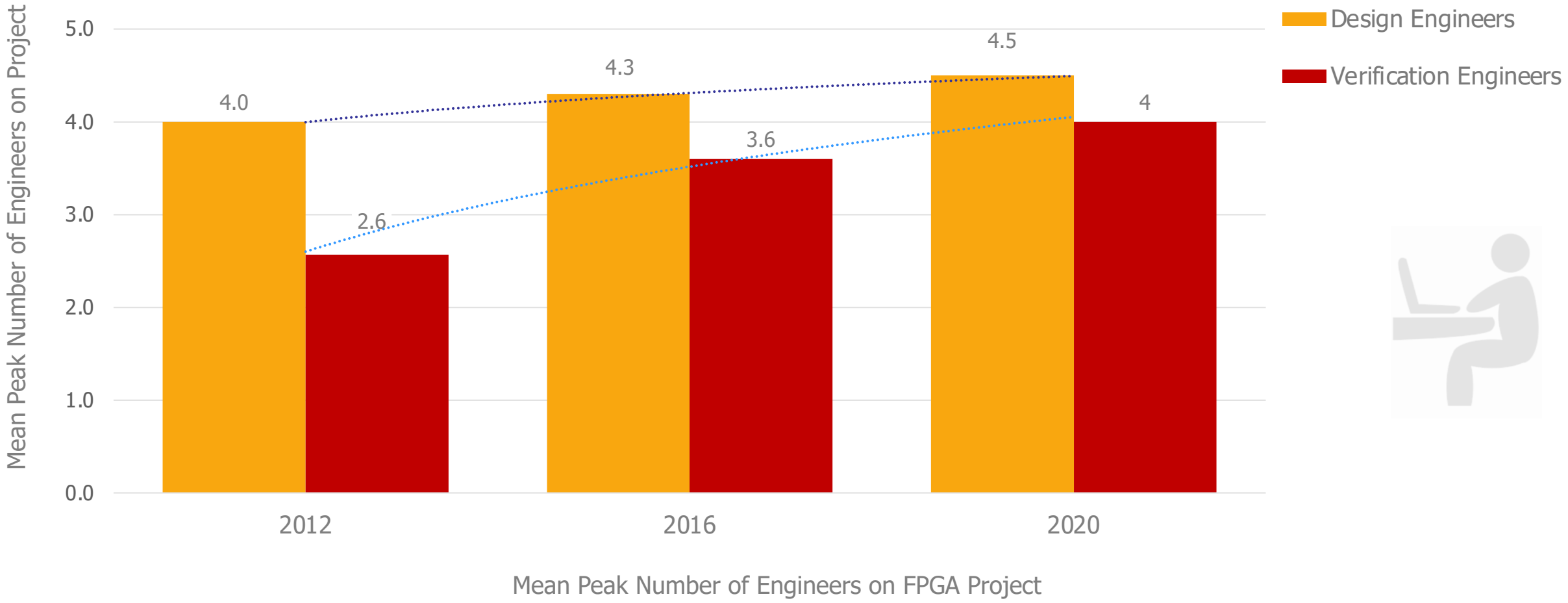
Mean Peak Number of Engineers By ASIC/IC Design Size



Mean Peak Number of ASIC Engineers by Design Size

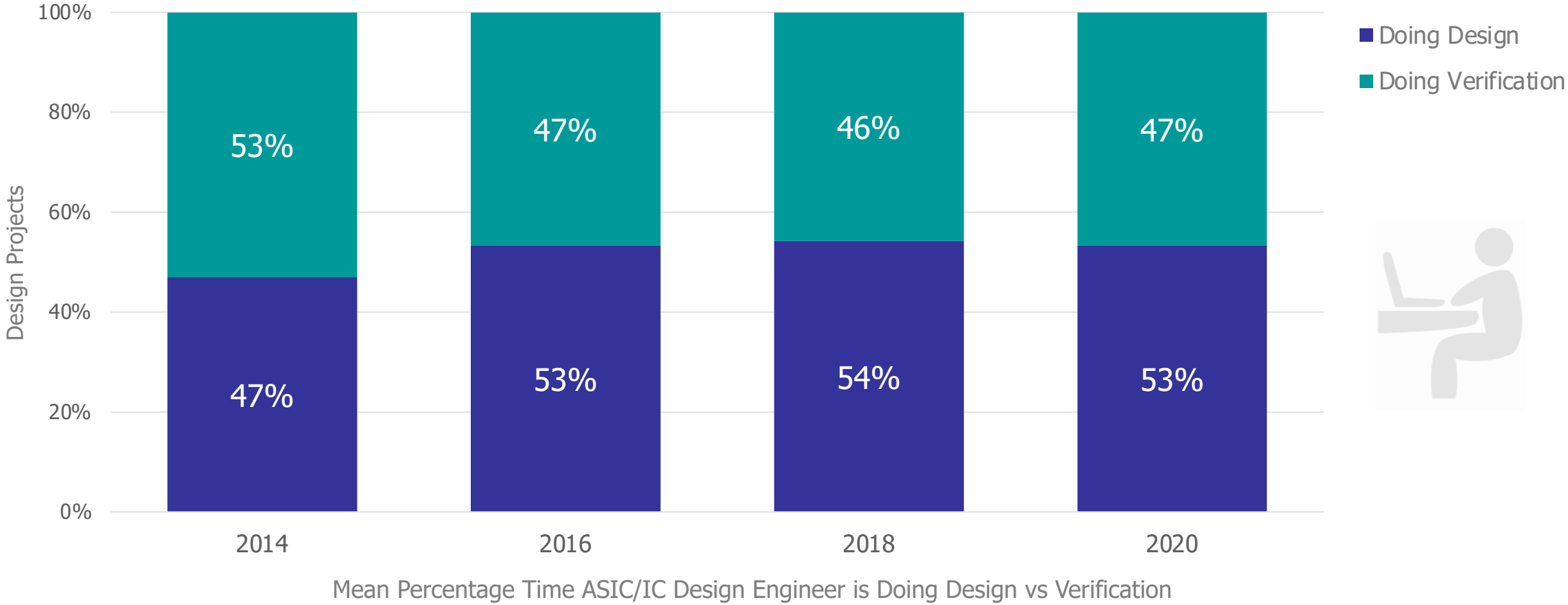
Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

Mean Peak Number of Engineers on a FPGA Project



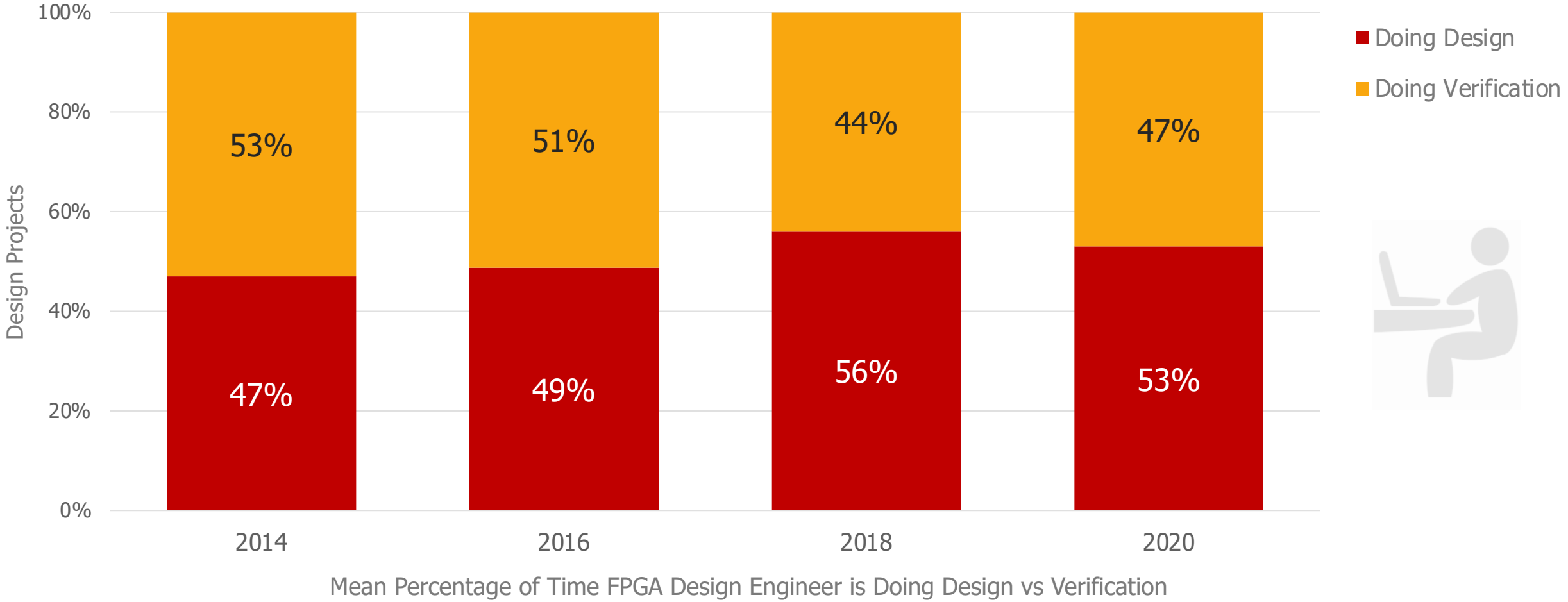
Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

Mean Time ASIC/IC Design Engineer is Doing Design vs Verification



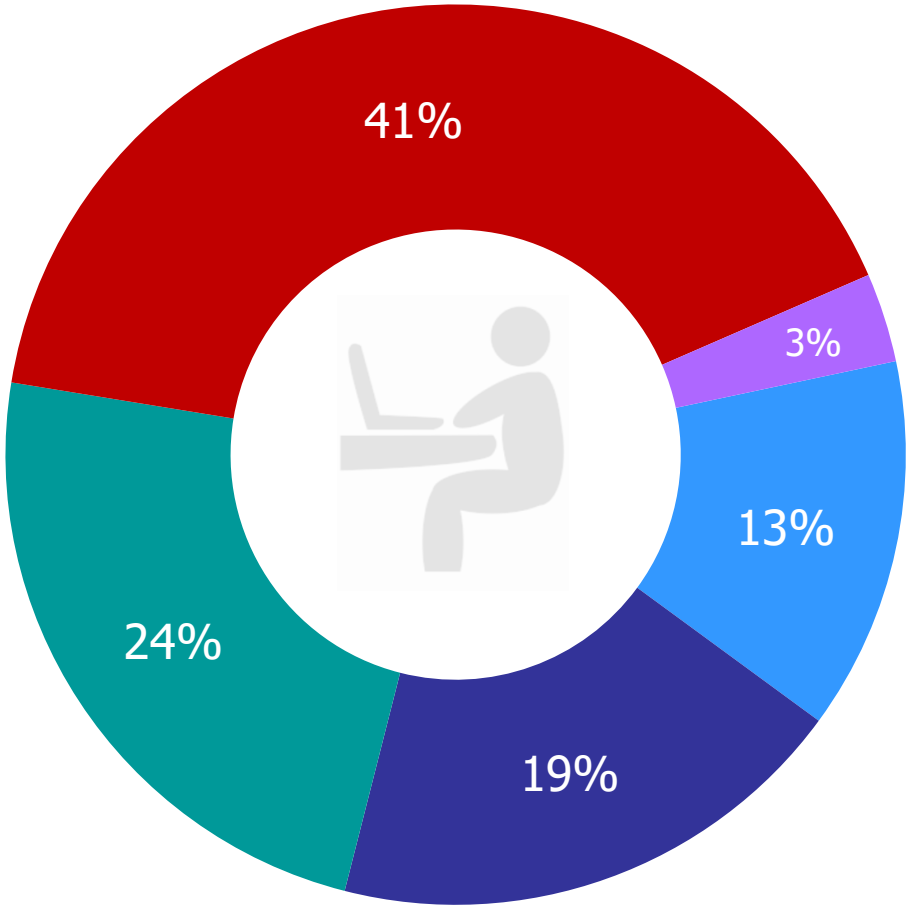
Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

Mean Time Design FPGA Engineer is Doing Design vs Verification



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

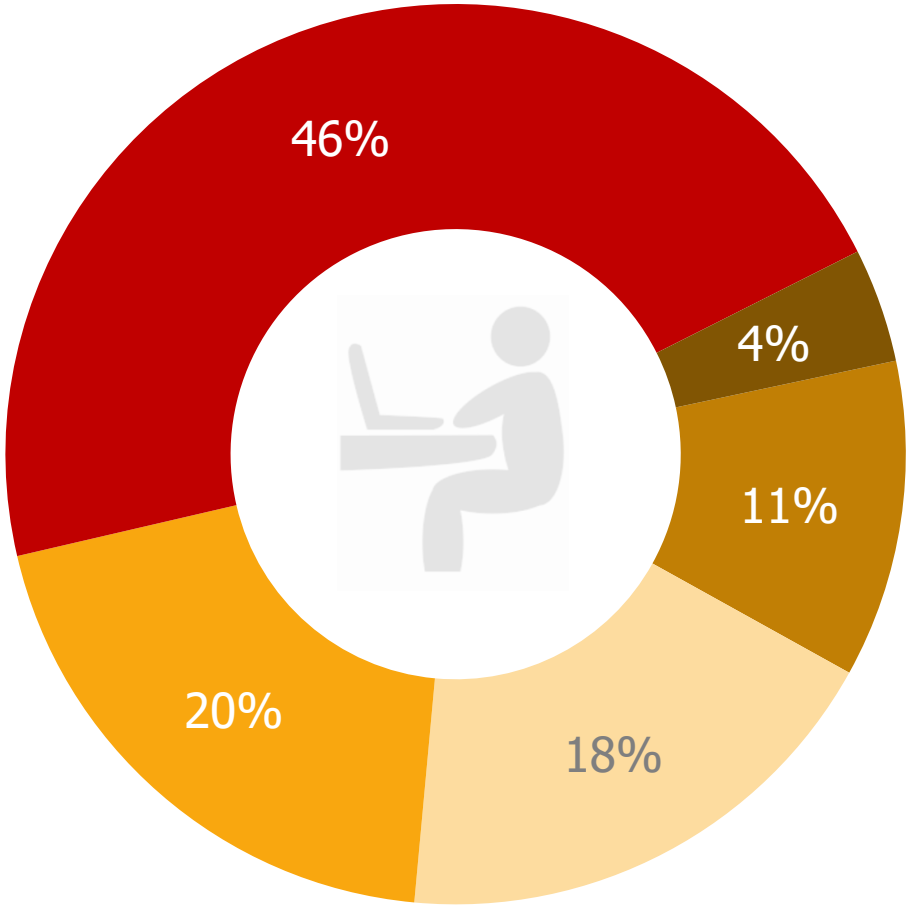
Where ASIC/IC Verification Engineers Spend Their Time



- Test Planning
- Testbench Development
- Creating Test and Running Simulation
- Debug
- Other

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

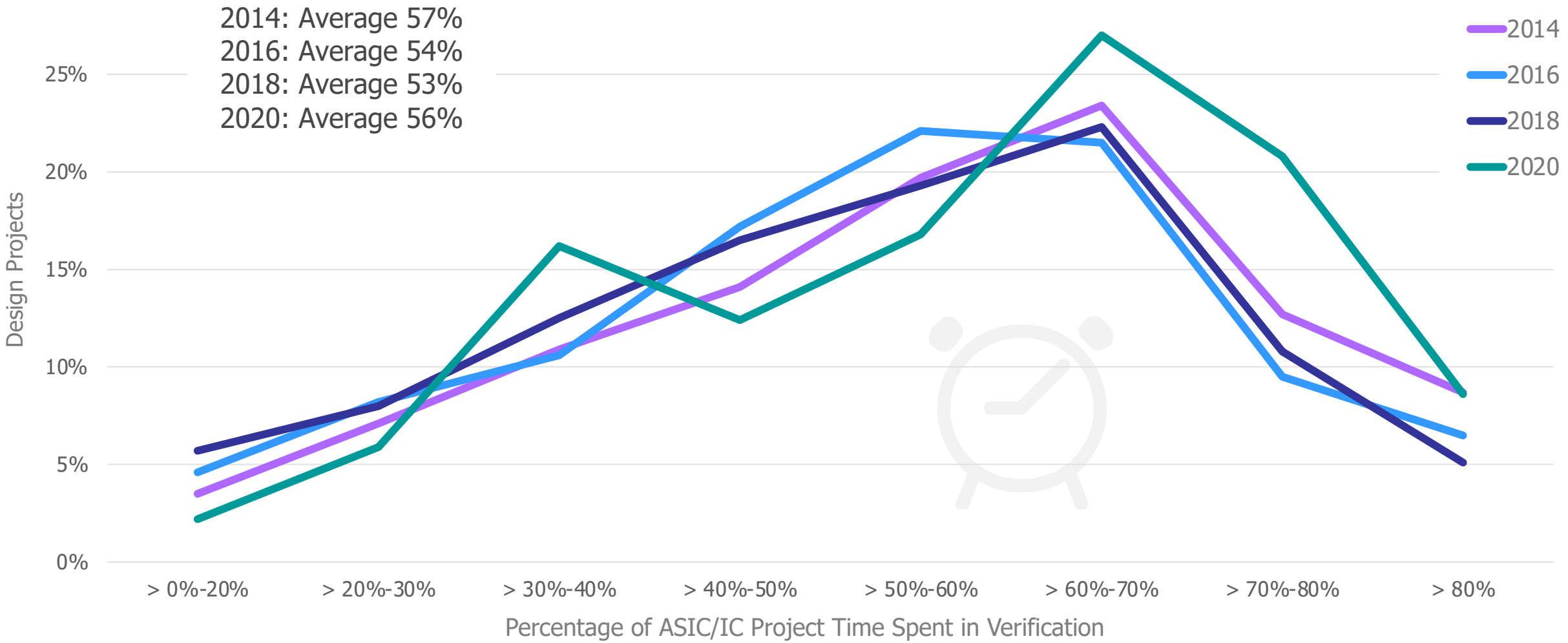
Where FPGA Verification Engineers Spend Their Time



- Test Planning
- Testbench Development
- Creating Test and Running Simulation
- Debug
- Other

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

Percentage of ASIC/IC Project Time Spent in Verification



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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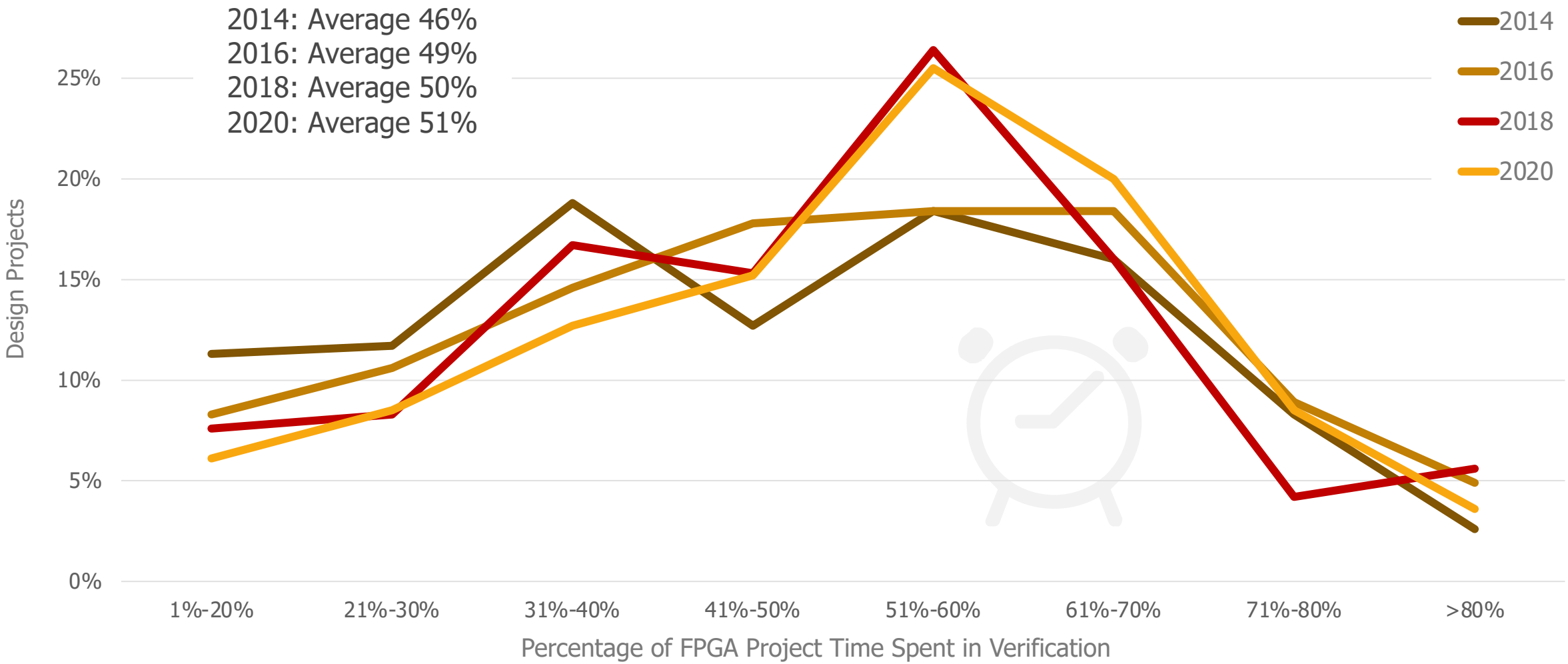
Percentage of FPGA Project Time Spent in Verification



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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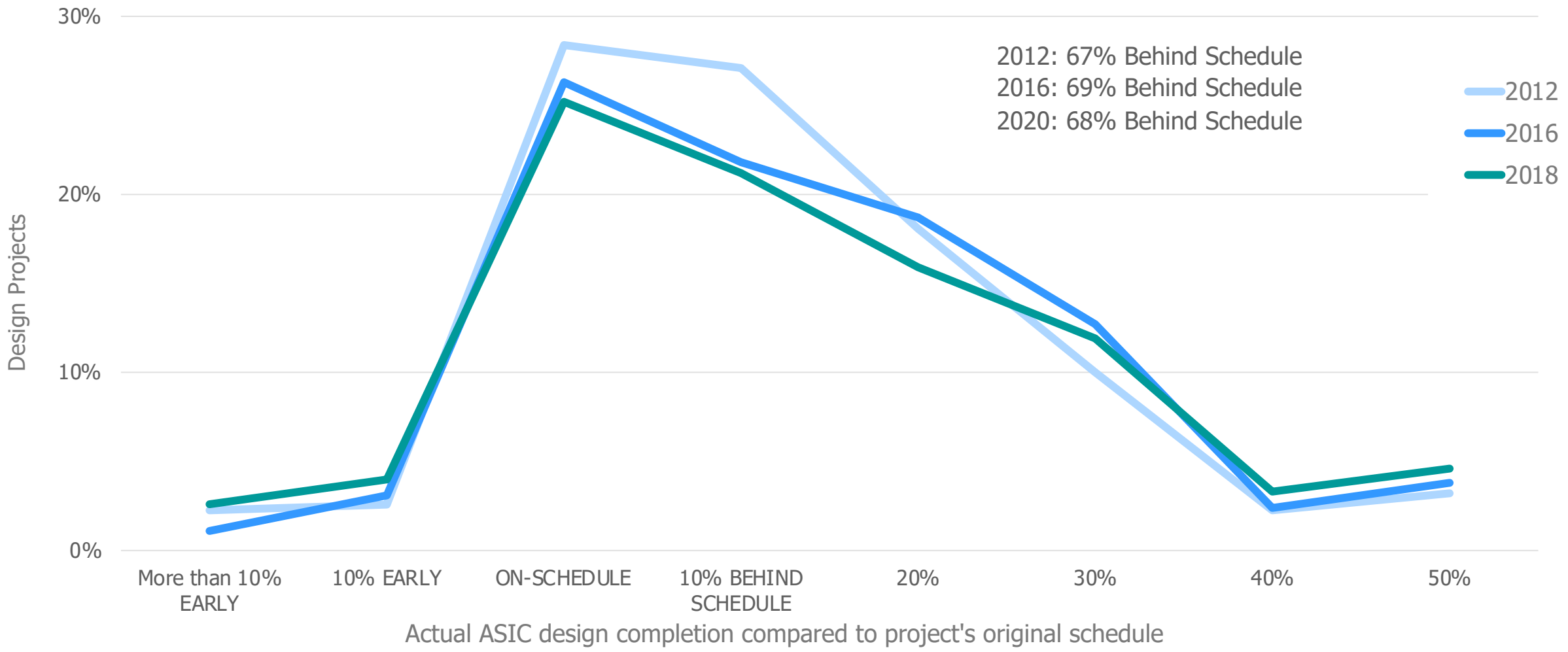
VERIFICATION RESULTS

ASIC Completion to Project's Original Schedule



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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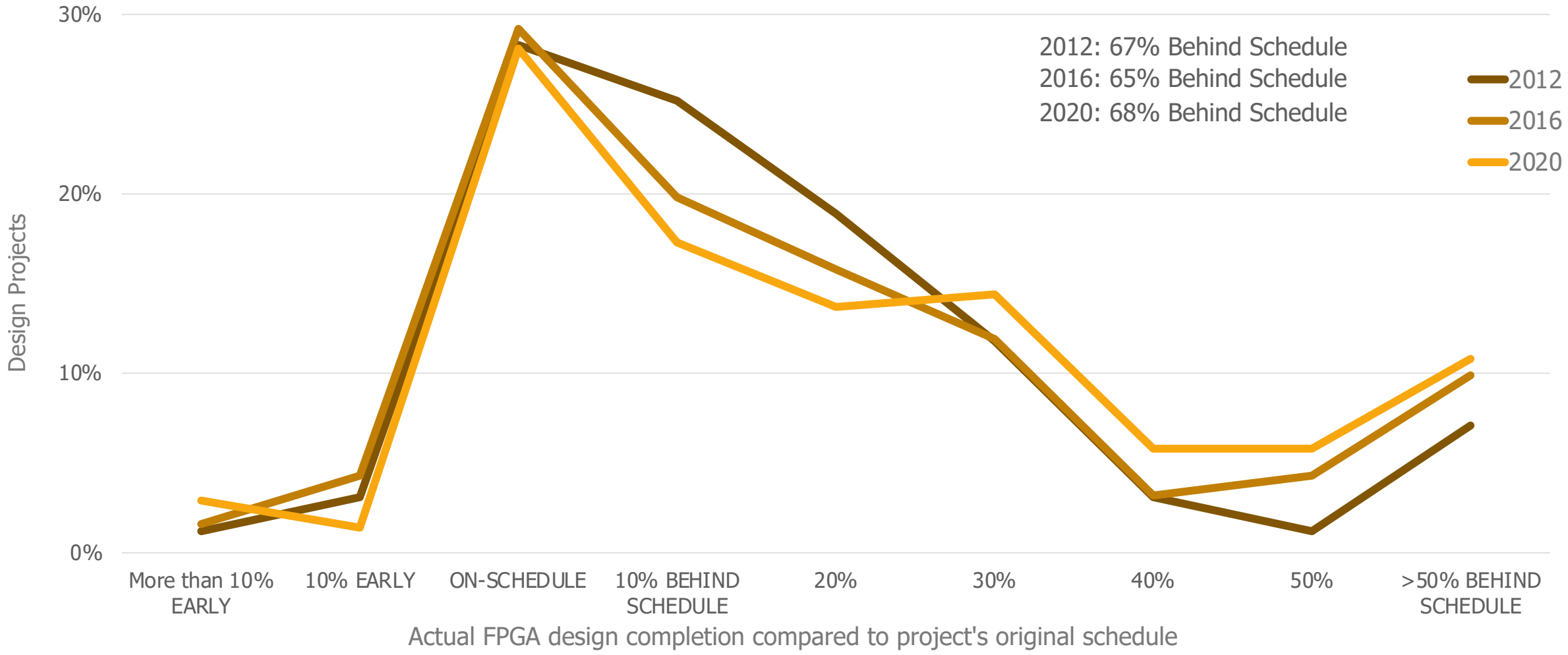
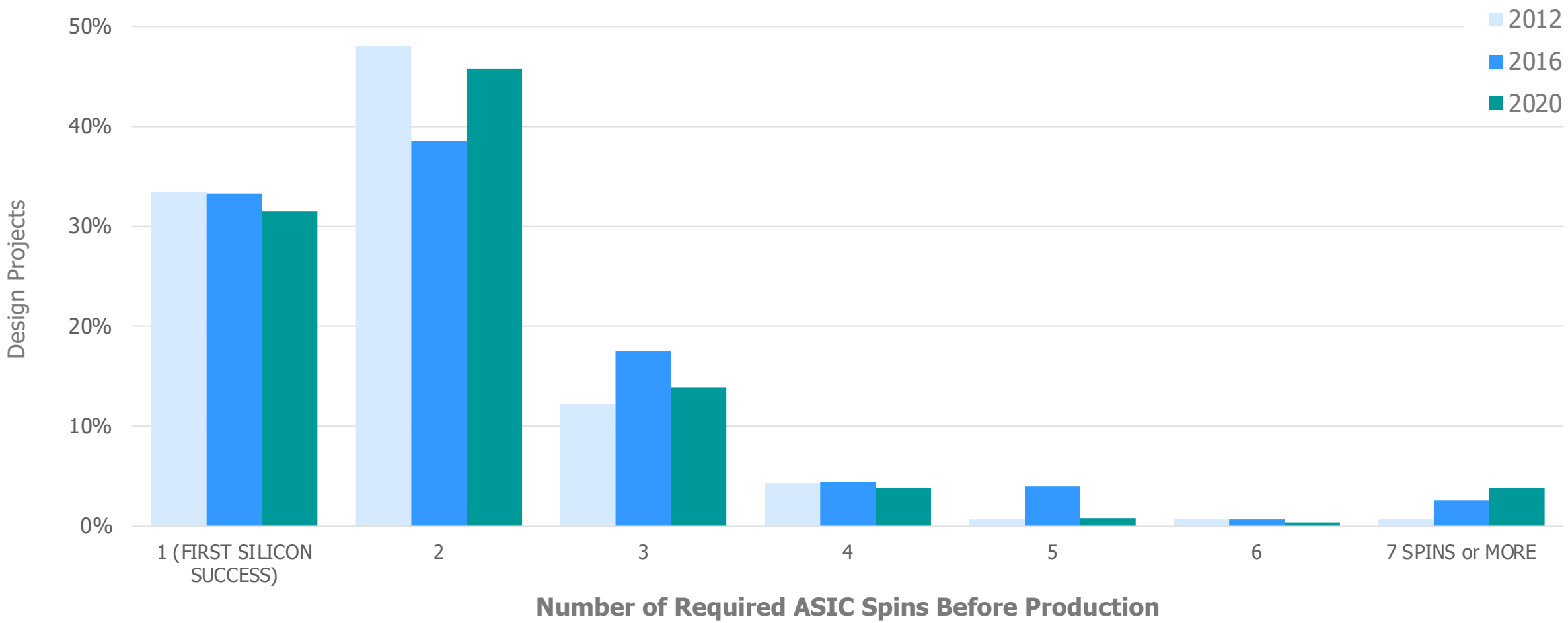
FPGA Completion to Project's Original Schedule



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

ASIC Number of Required Spins Before Production



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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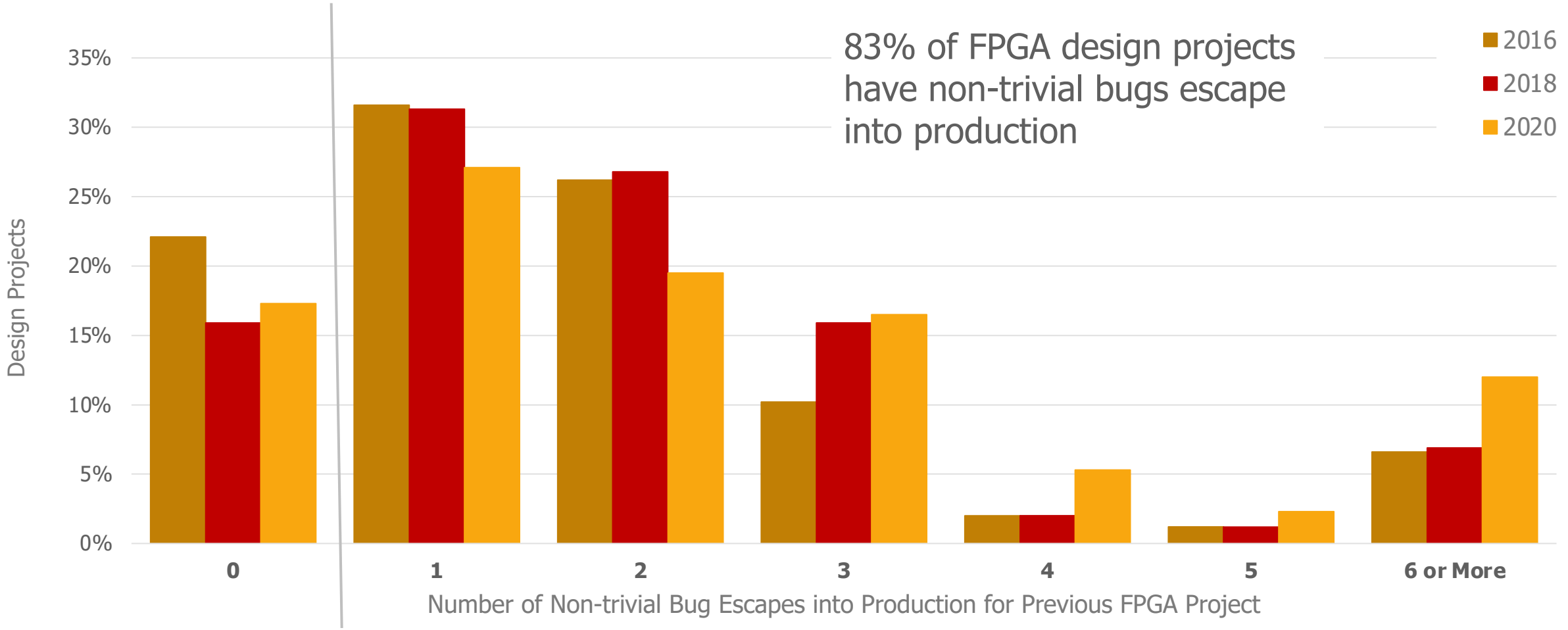
Number of Non-trivial FPGA Bug Escapes into Production



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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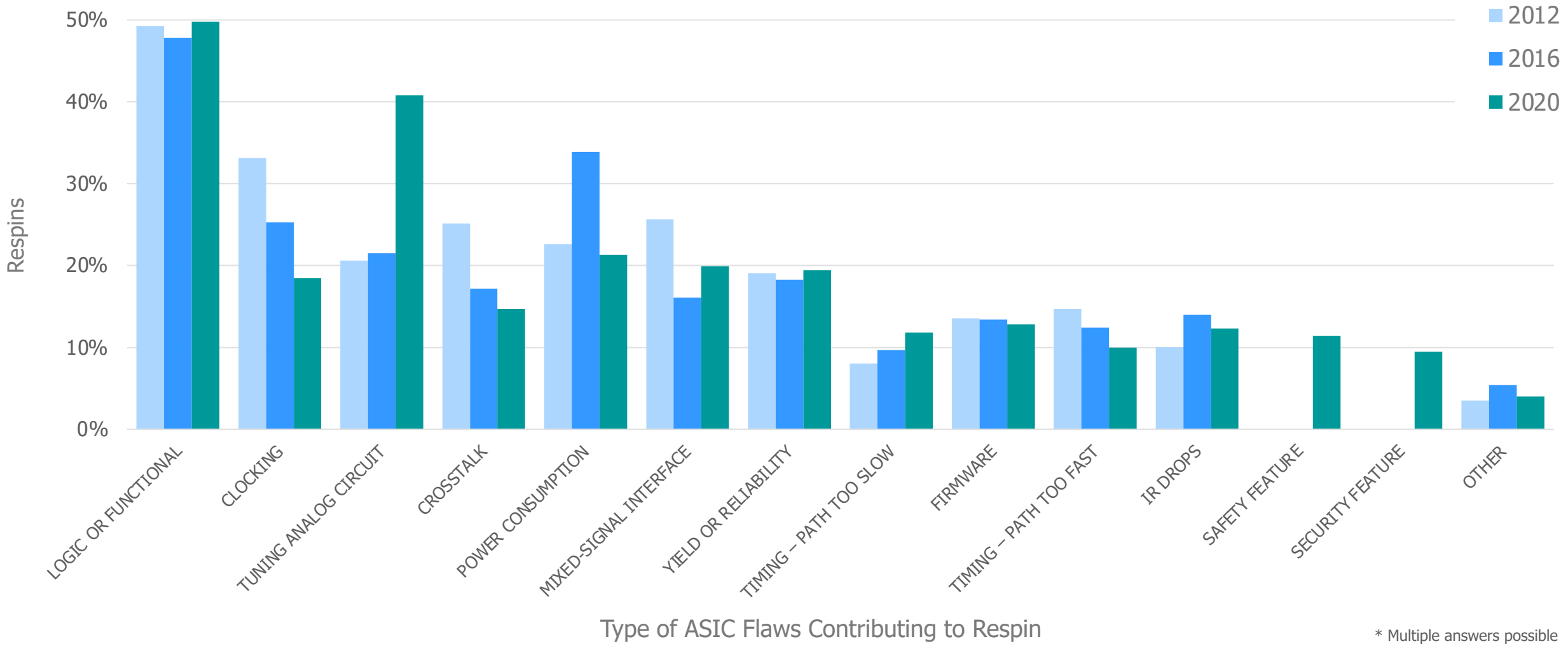
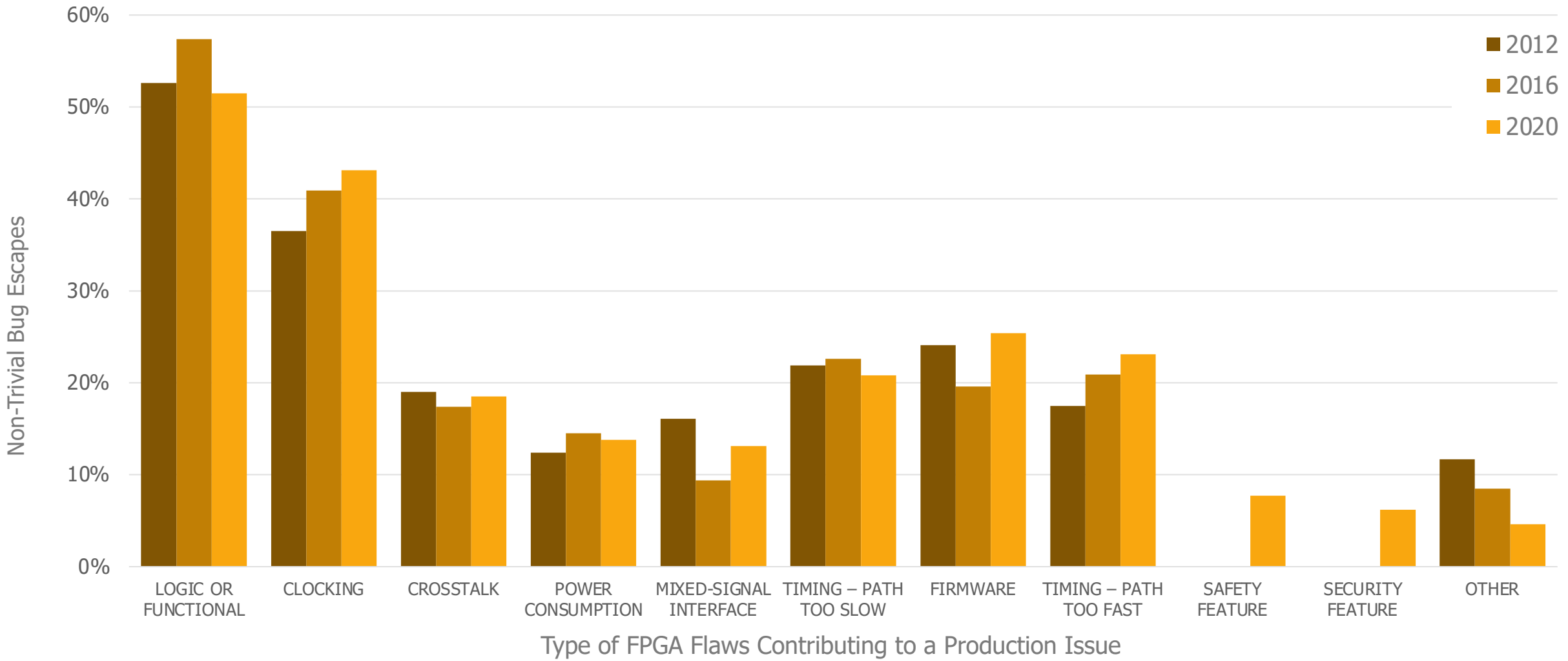
ASIC Type of Flaws Contributing to Respin



* Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

FPGA Type of Flaws Contributing to a Production Issue



* Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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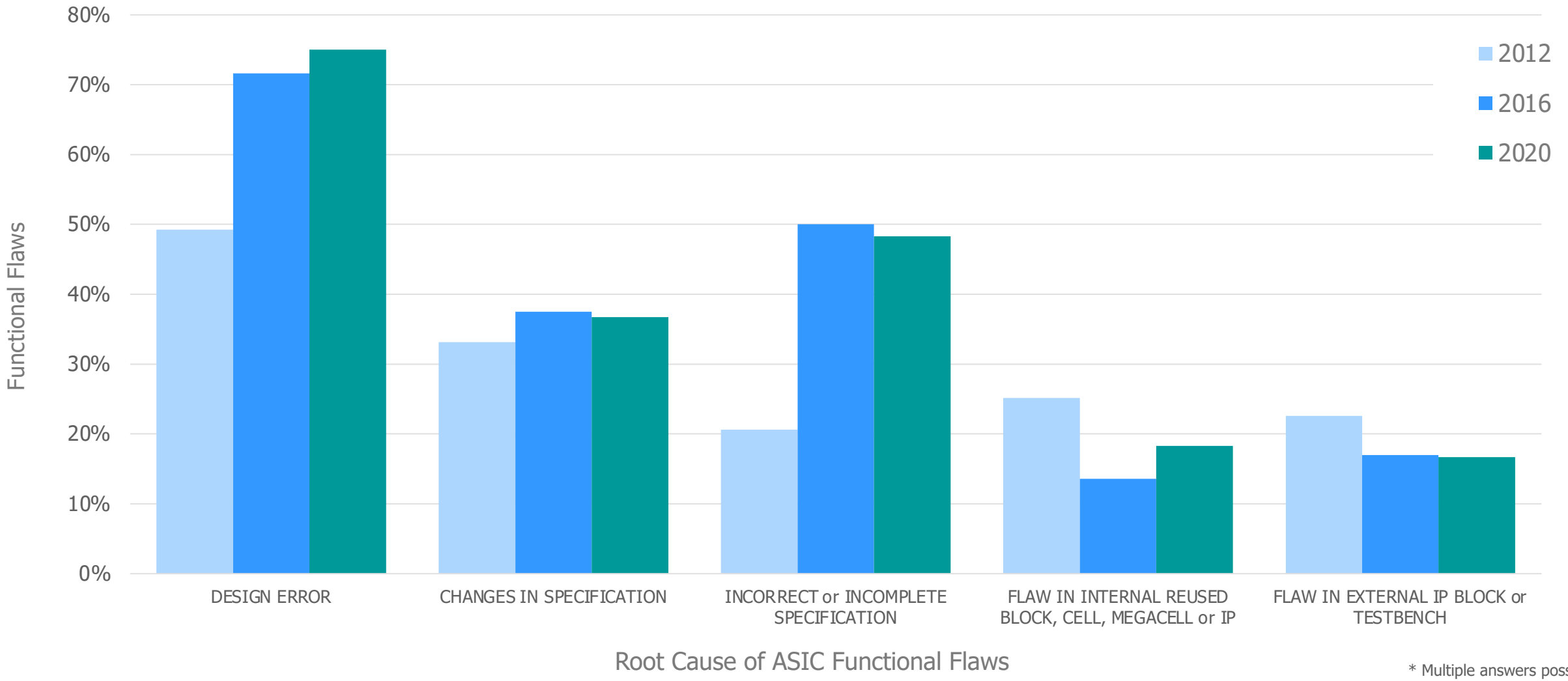
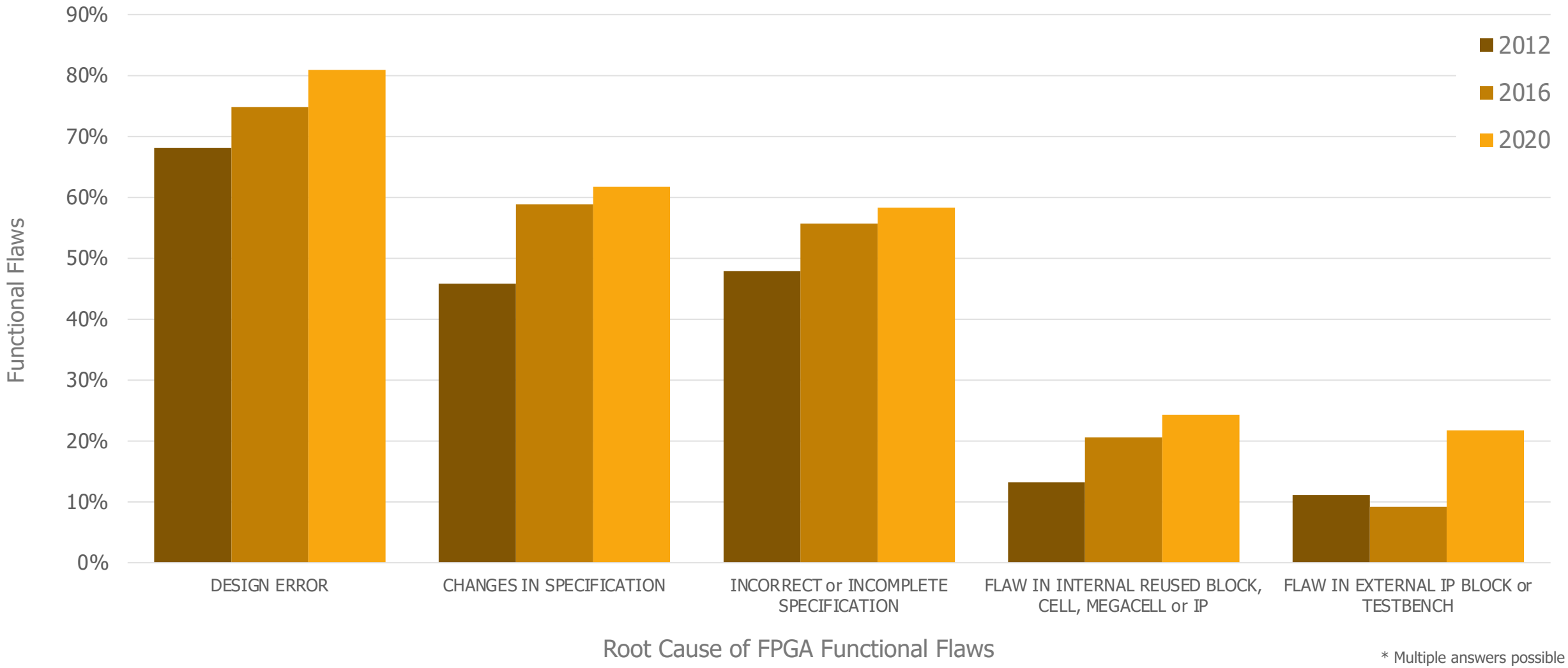
Root Cause of ASIC Functional Flaws



* Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

Root Cause of FPGA Functional Flaws

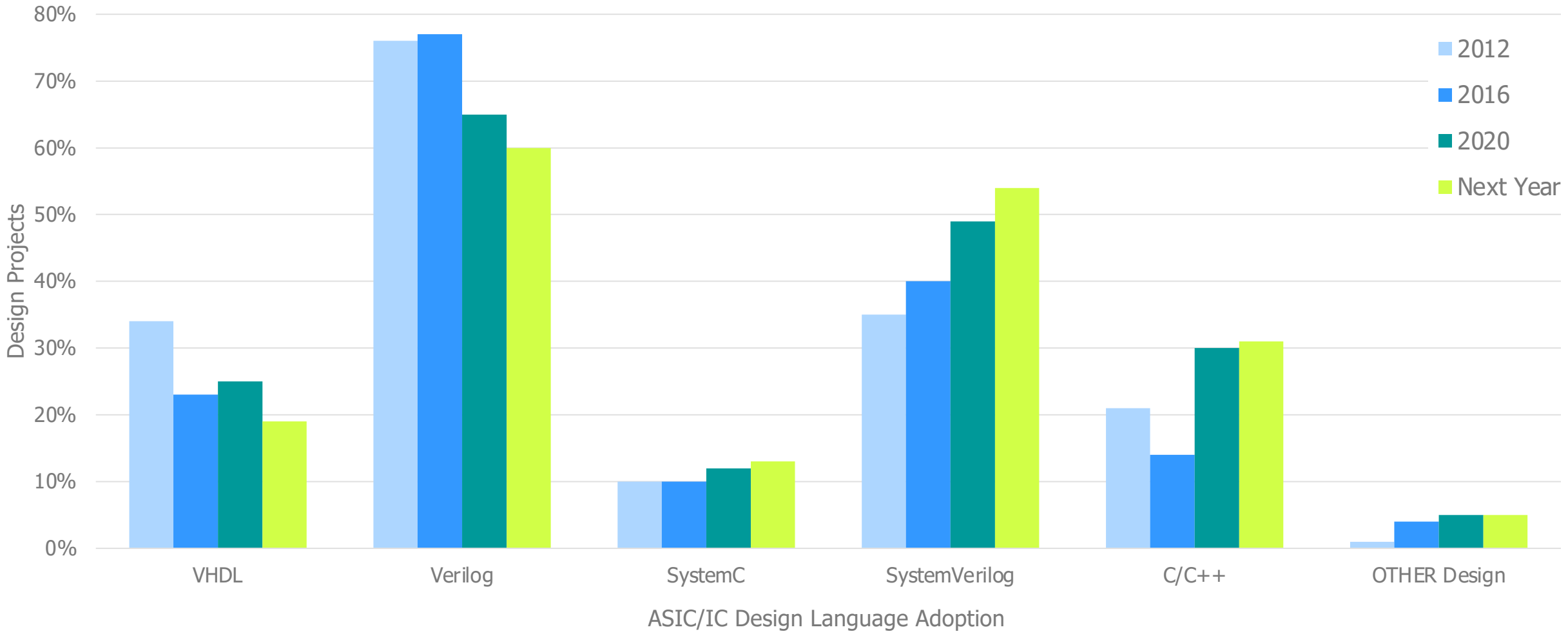


* Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

LANGUAGES & METHODOLOGIES

ASIC/IC Design Language Adoption Next Twelve Months



** Multiple answers possible

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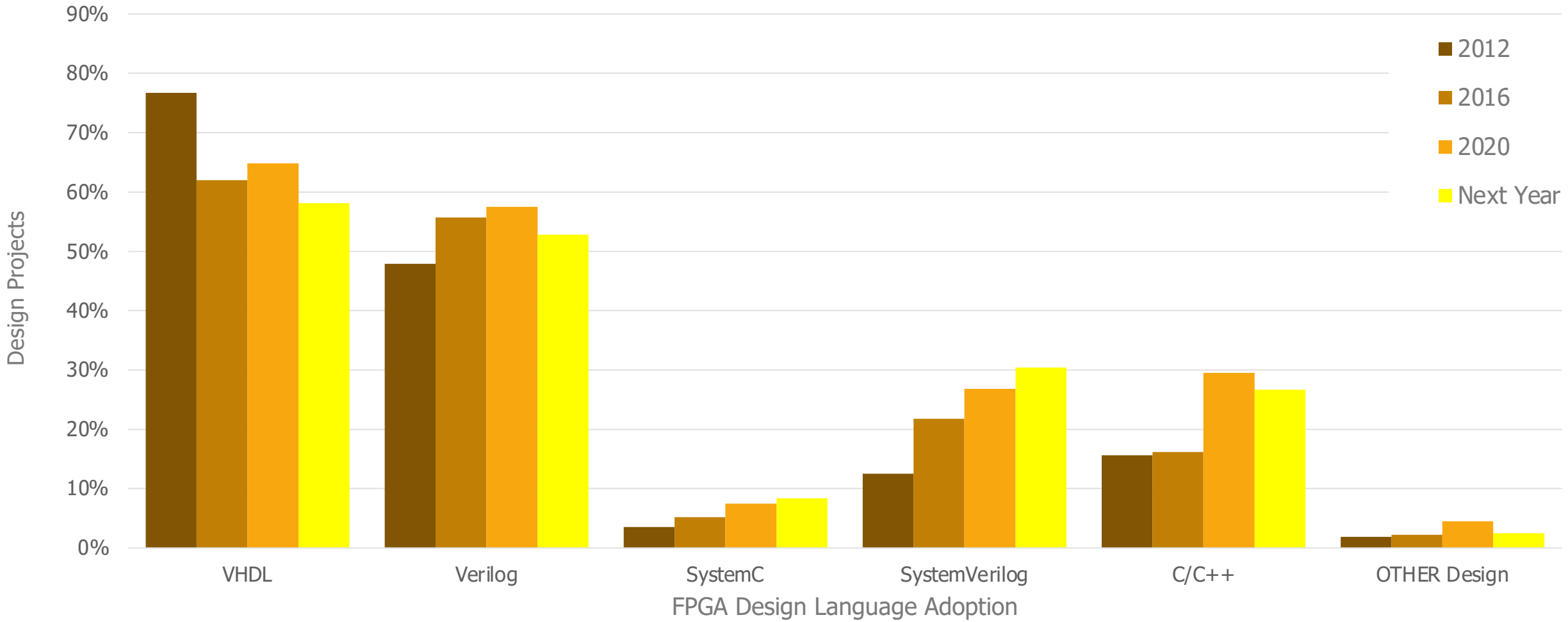
FPGA Design Language Adoption Next Twelve Months



* Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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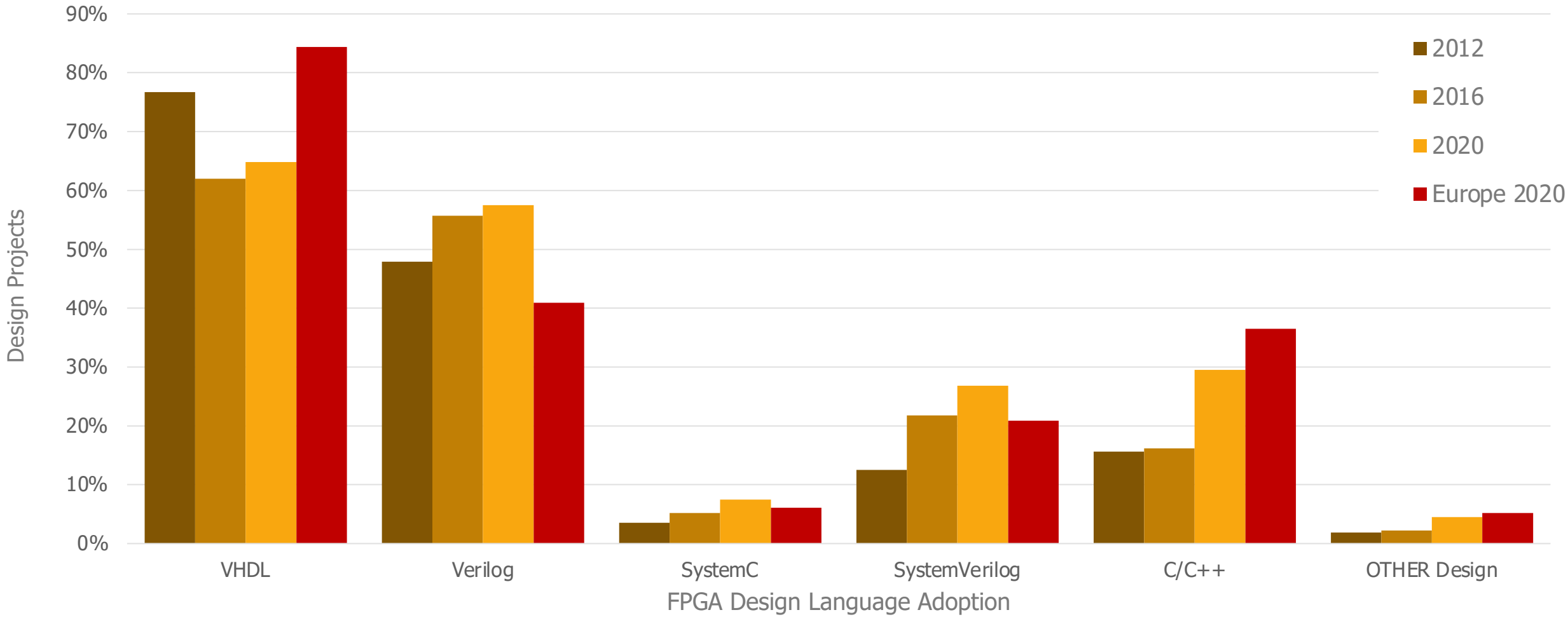
FPGA Design Language Adoption in Europe



* Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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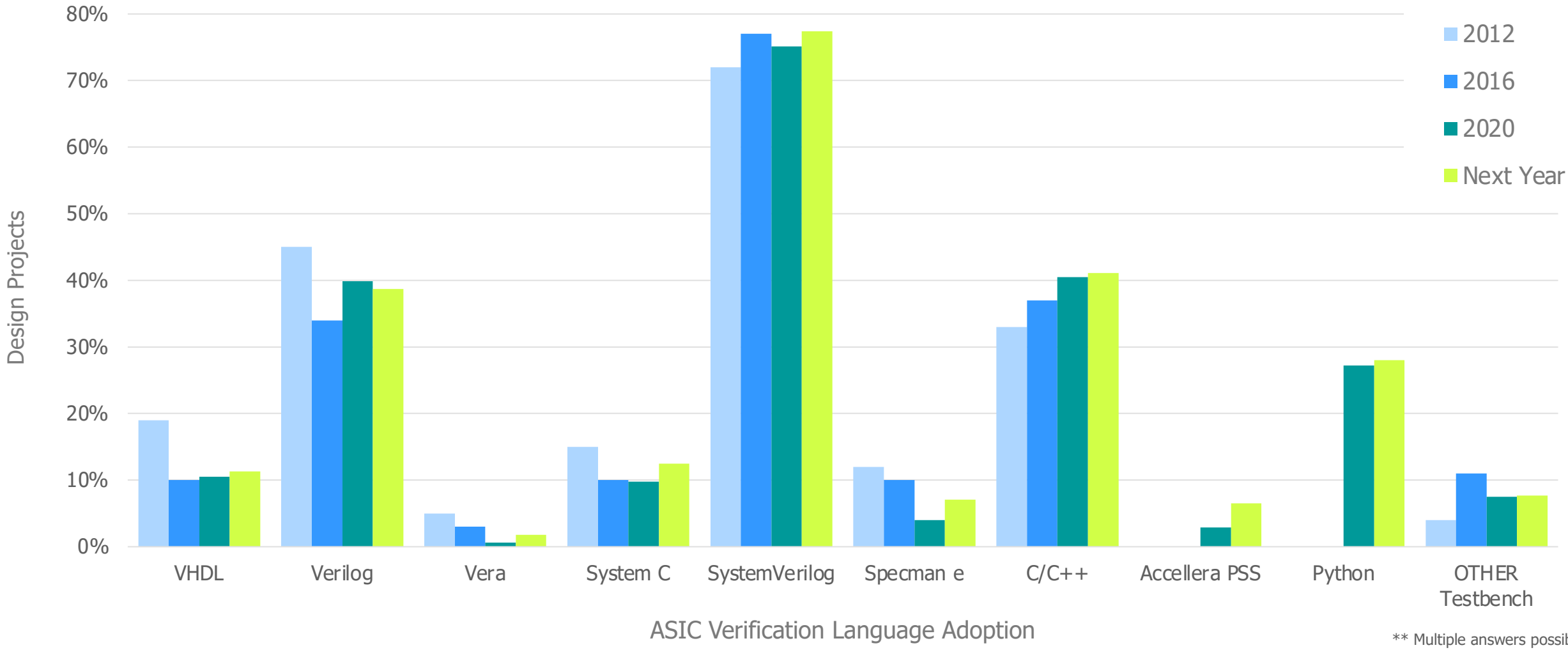
ASIC/IC Verification Language Adoption Next Twelve Months



** Multiple answers possible

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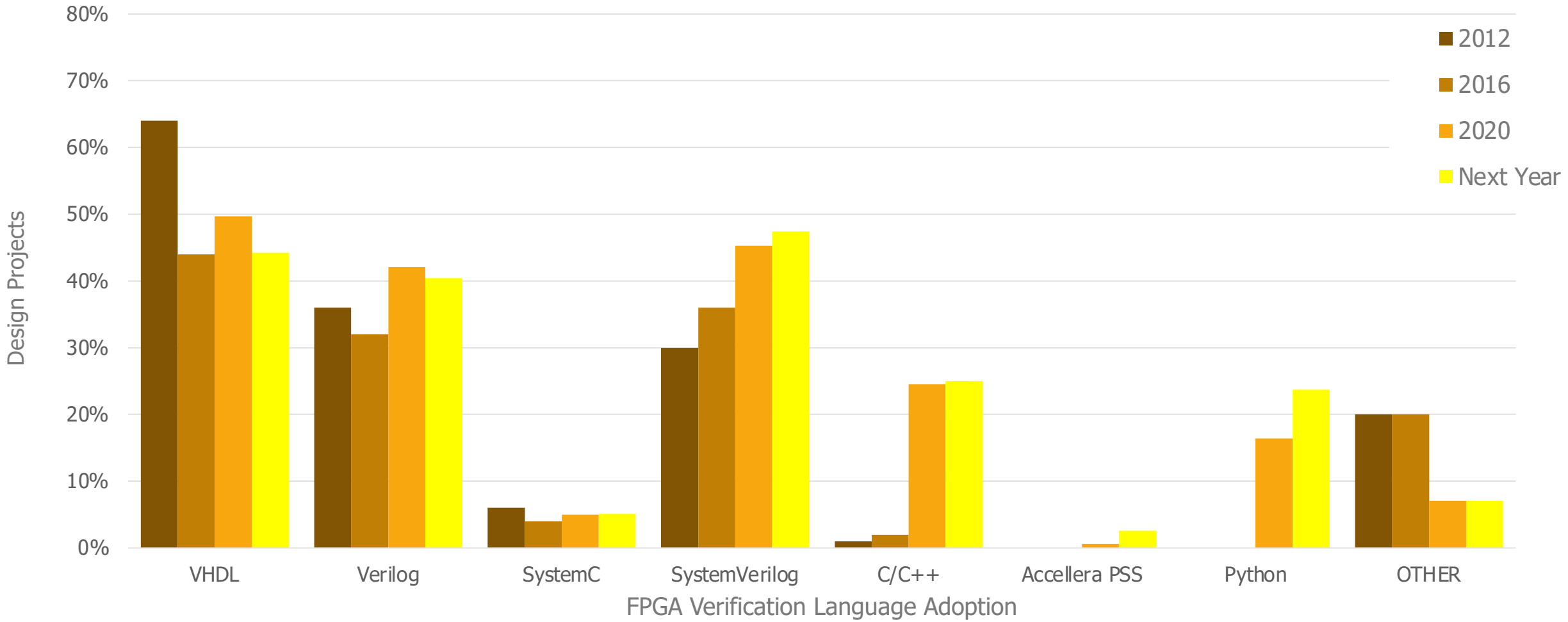
FPGA Verification Language Adoption Next Twelve Months



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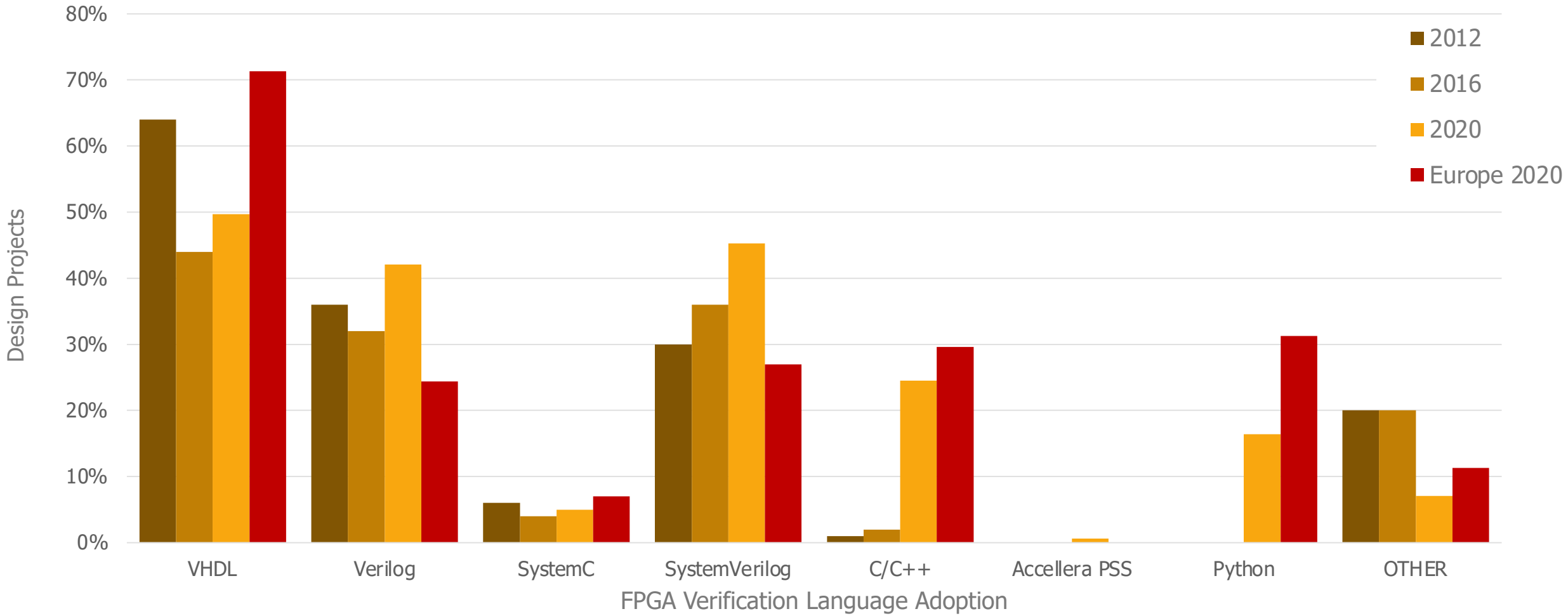
FPGA Verification Language Adoption Europe



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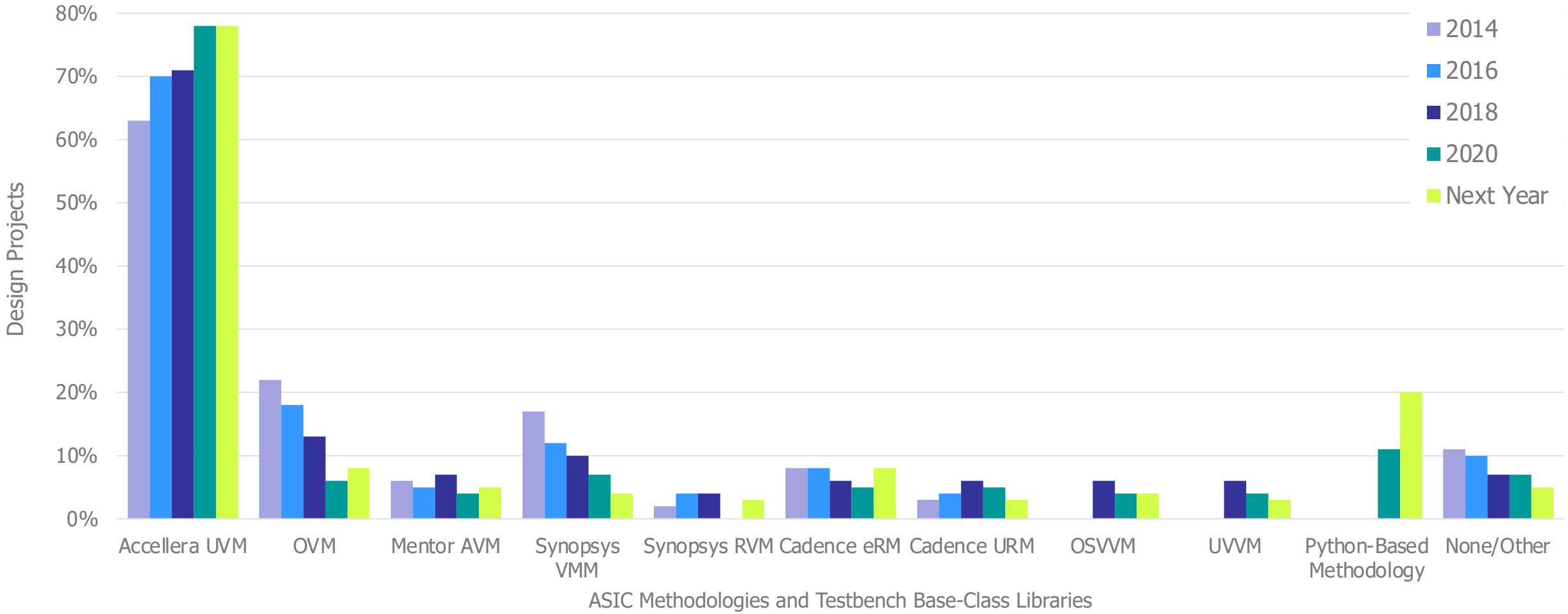
ASIC Methodologies and Testbench Base-Class Libraries



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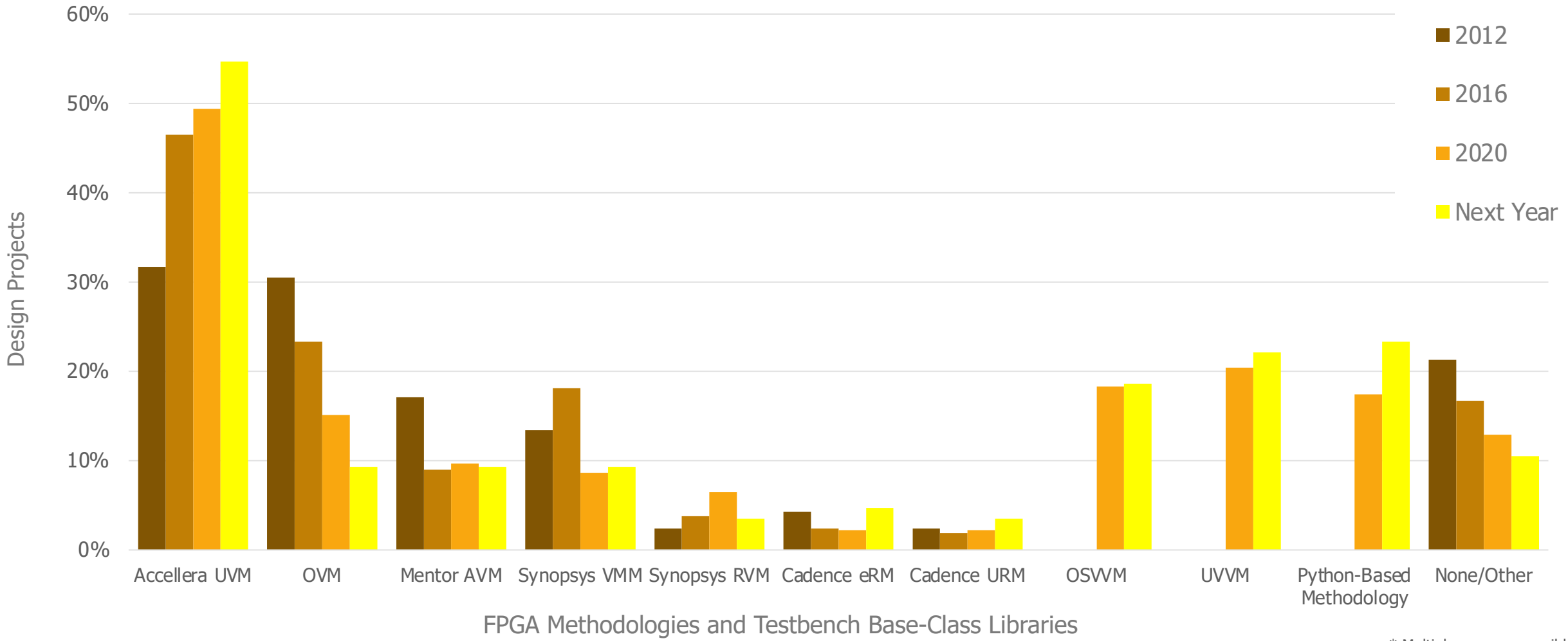
FPGA Methodologies and Testbench Base-Class Libraries



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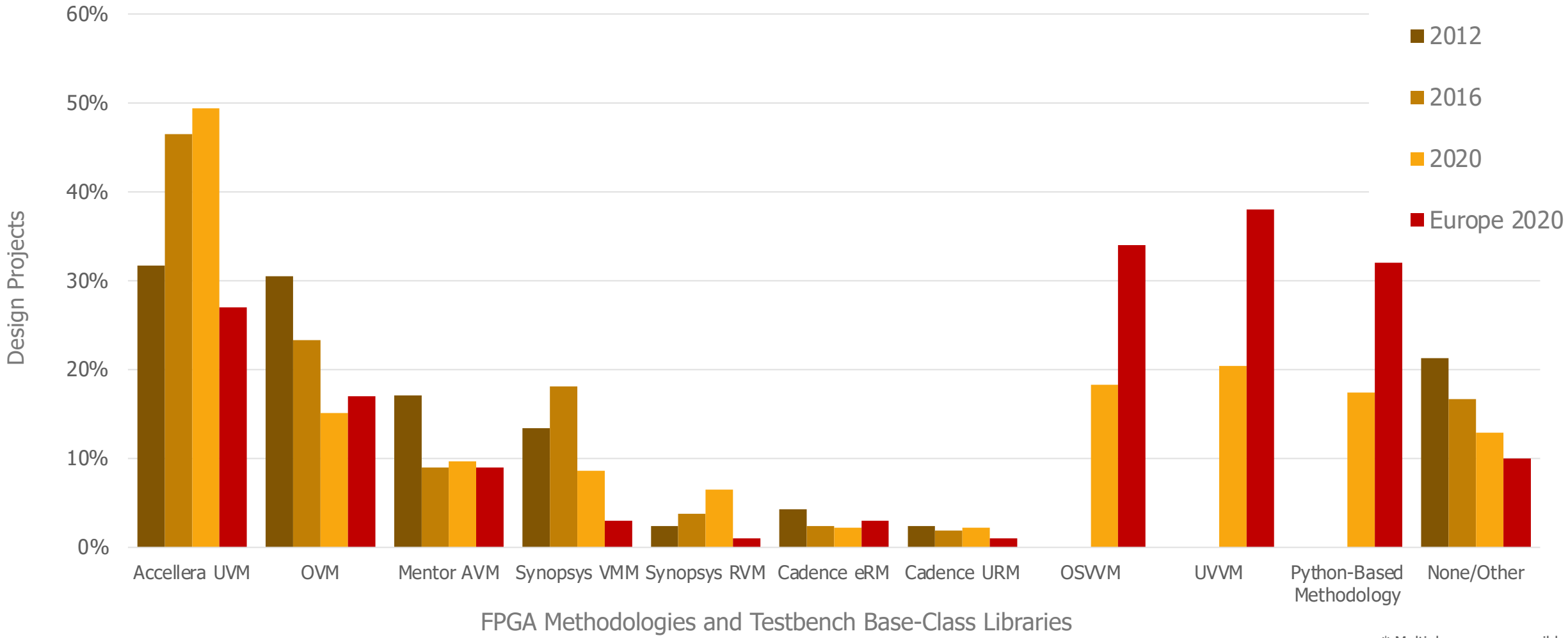
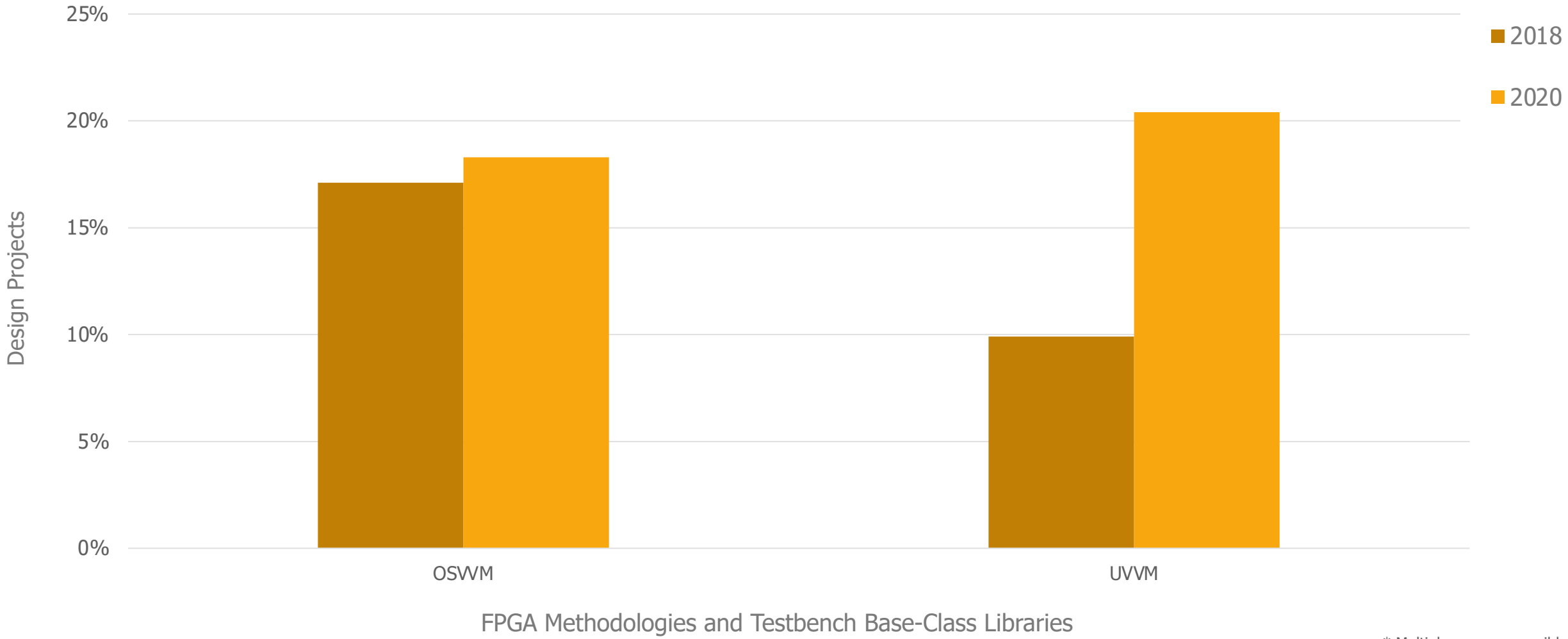
FPGA Methodologies and Testbench Base-Class Libraries Europe



* Multiple answers possible

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

FPGA OSVVM and UVVM Trends



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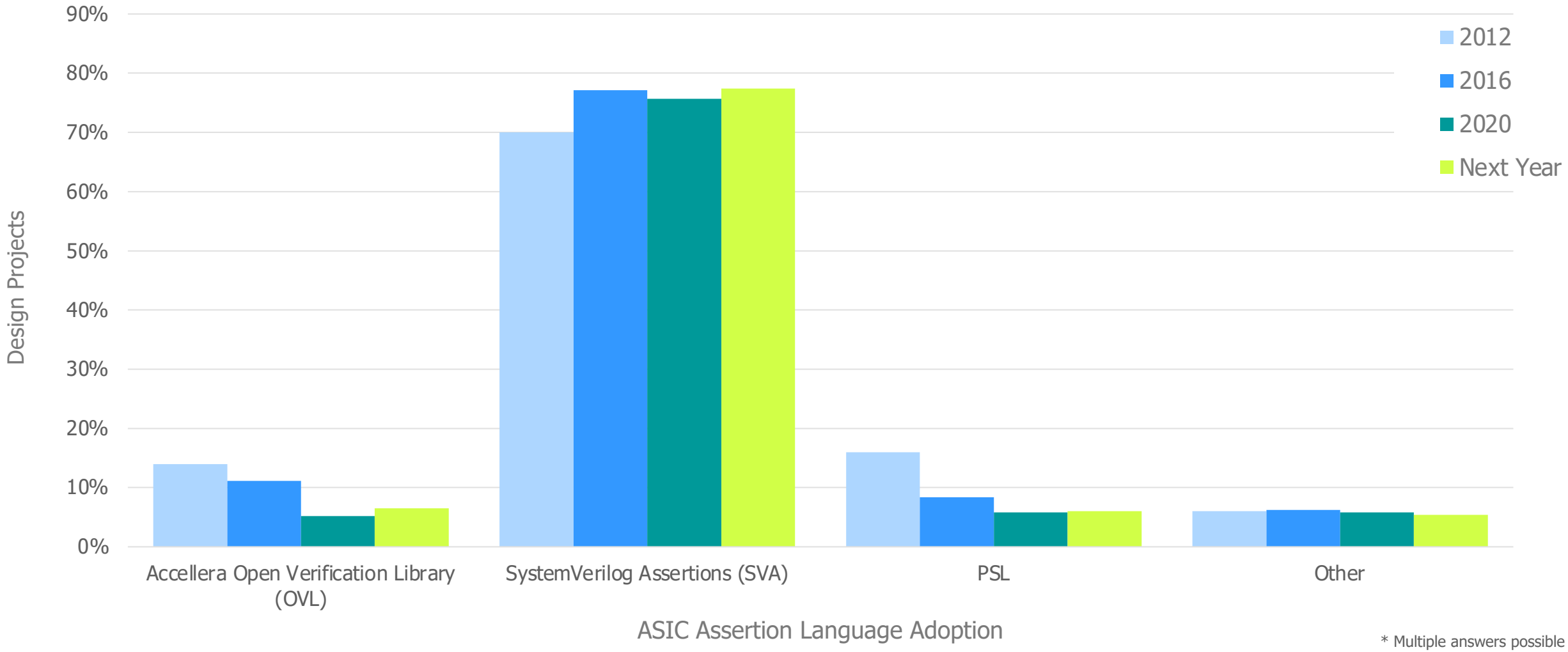
Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

ASIC Assertion Language Adoption Next Twelve Months



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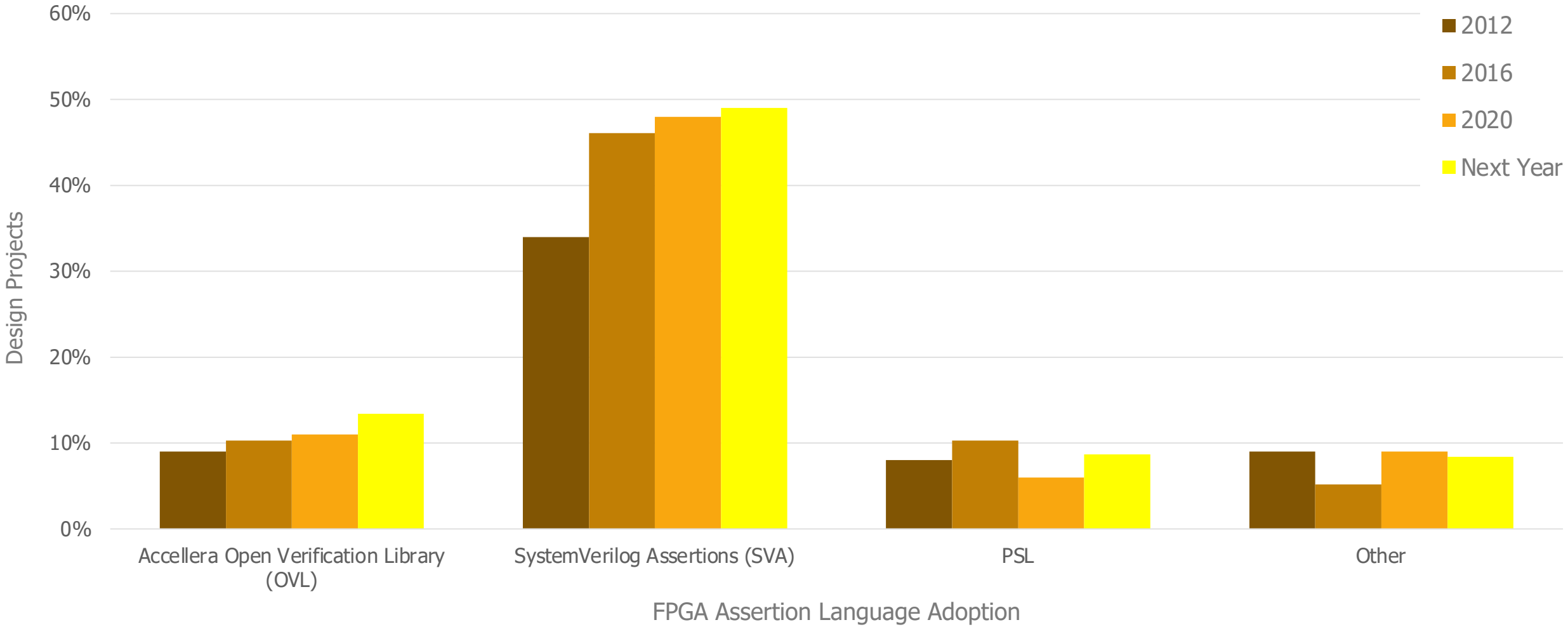
FPGA Assertion Language Adoption Next Twelve Months



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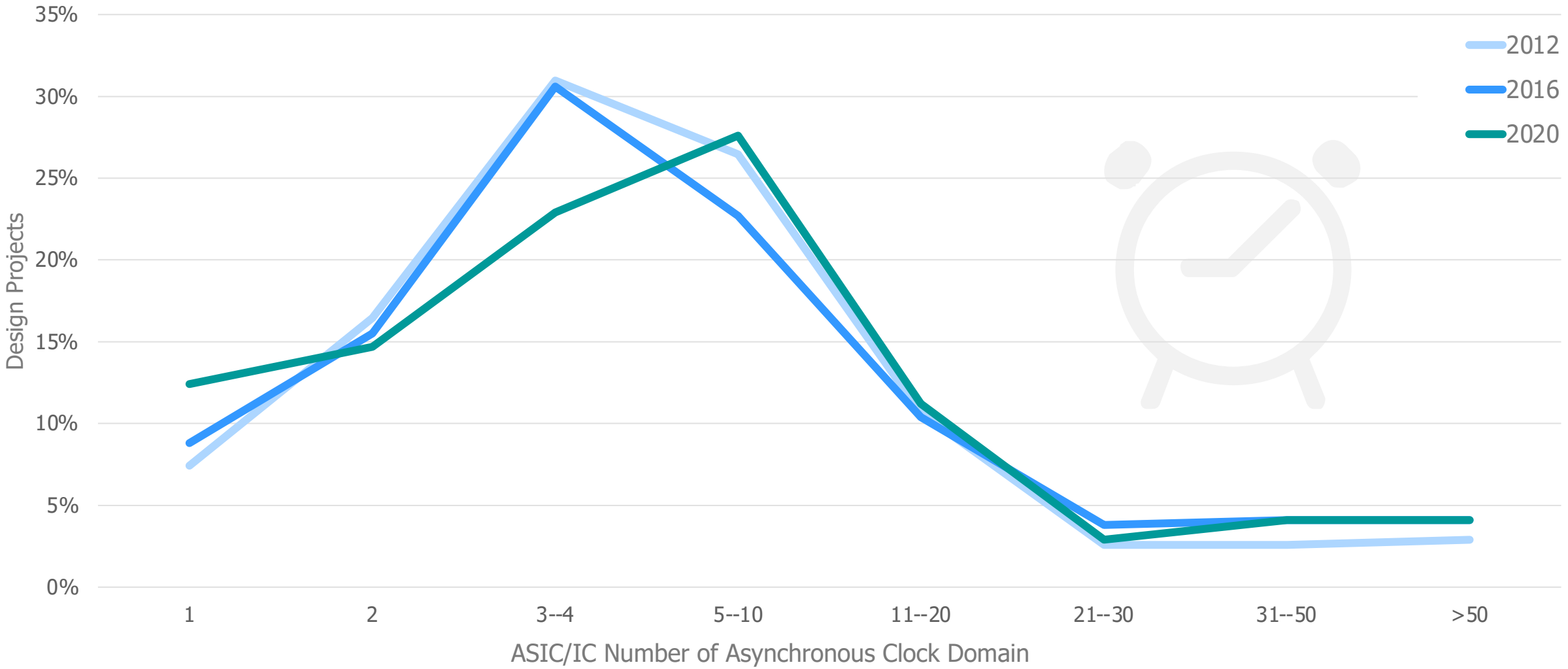
Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

POWER AND CLOCKING

ASIC/IC Number of Asynchronous Clock Domain



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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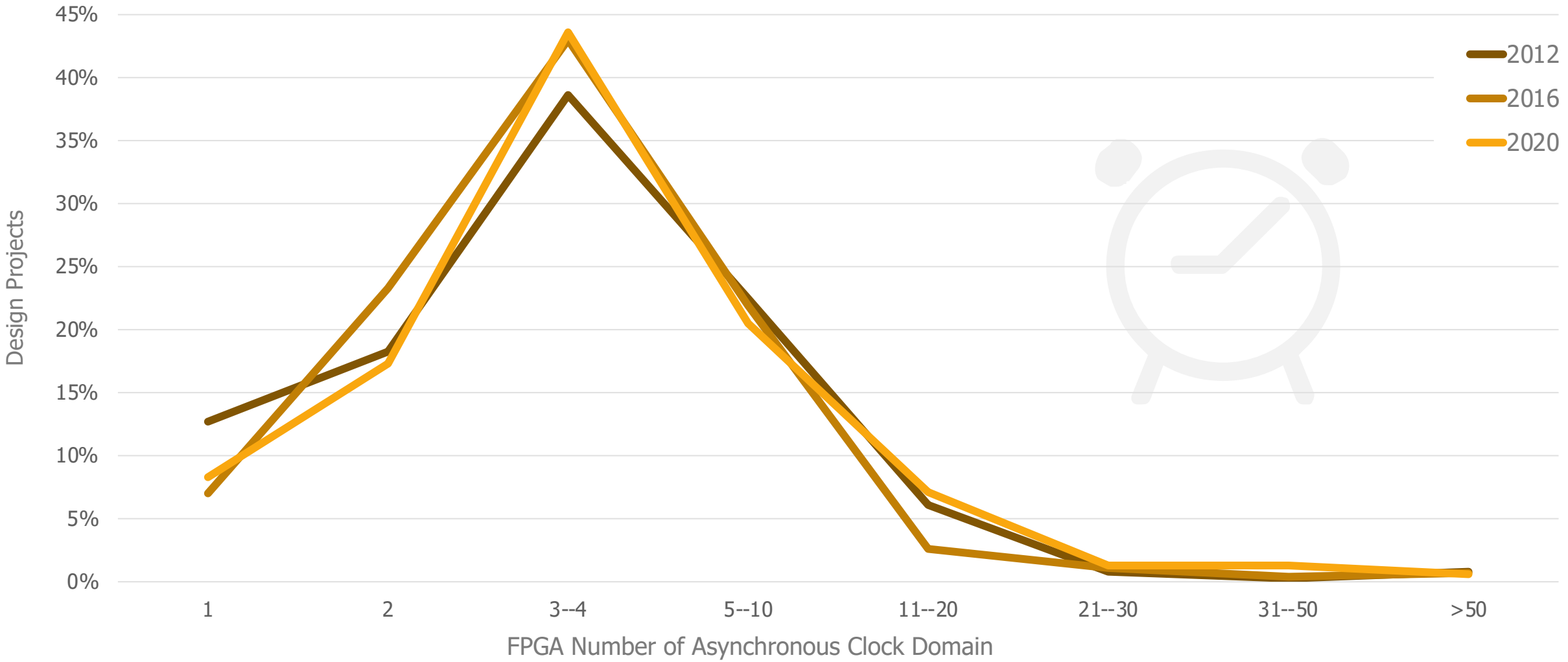
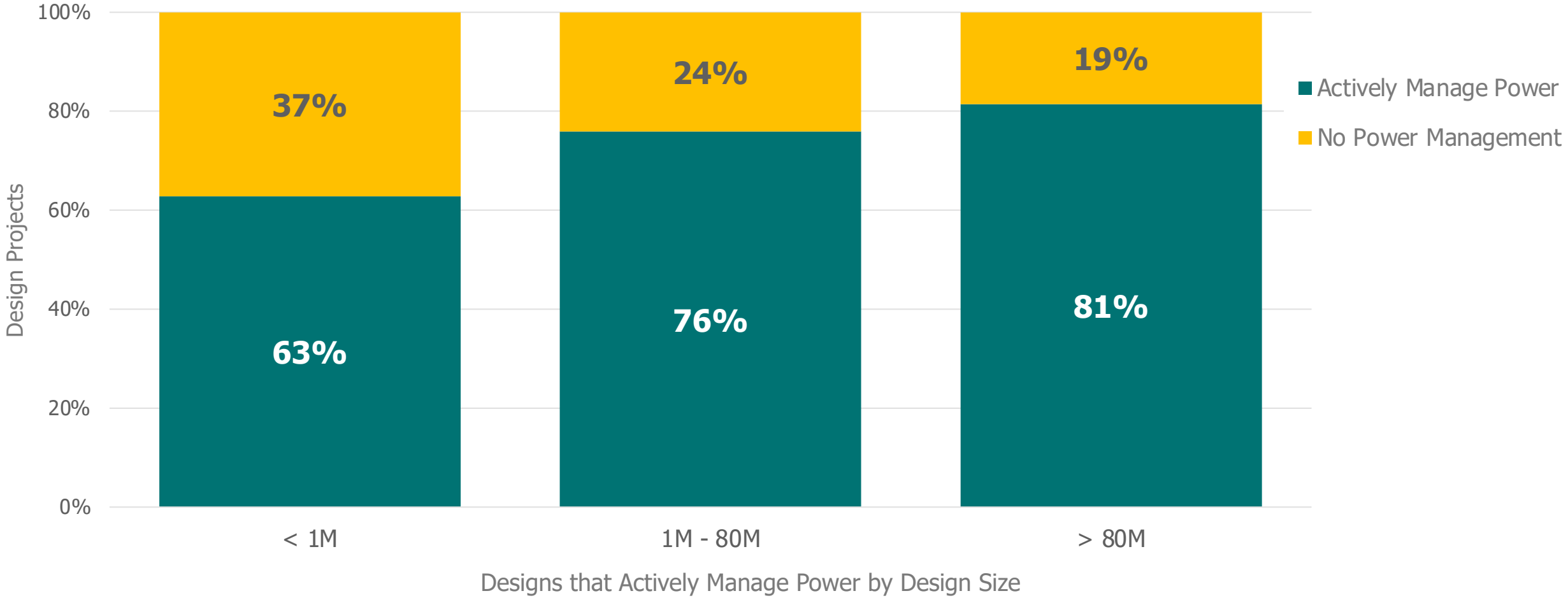
FPGA Number of Asynchronous Clock Domain



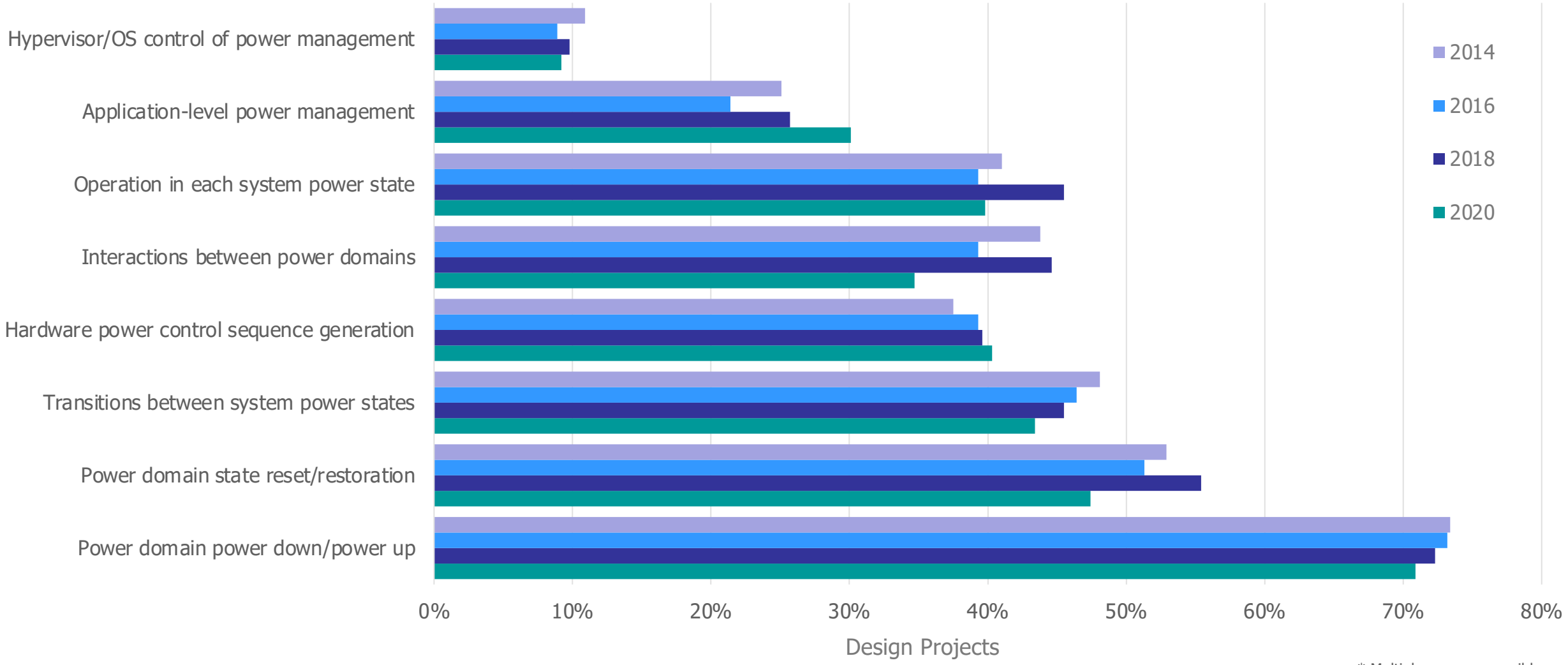
Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

ASIC/IC Actively Manage Power by Design Size



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

ASIC Power Management Features Verified



* Multiple answers possible

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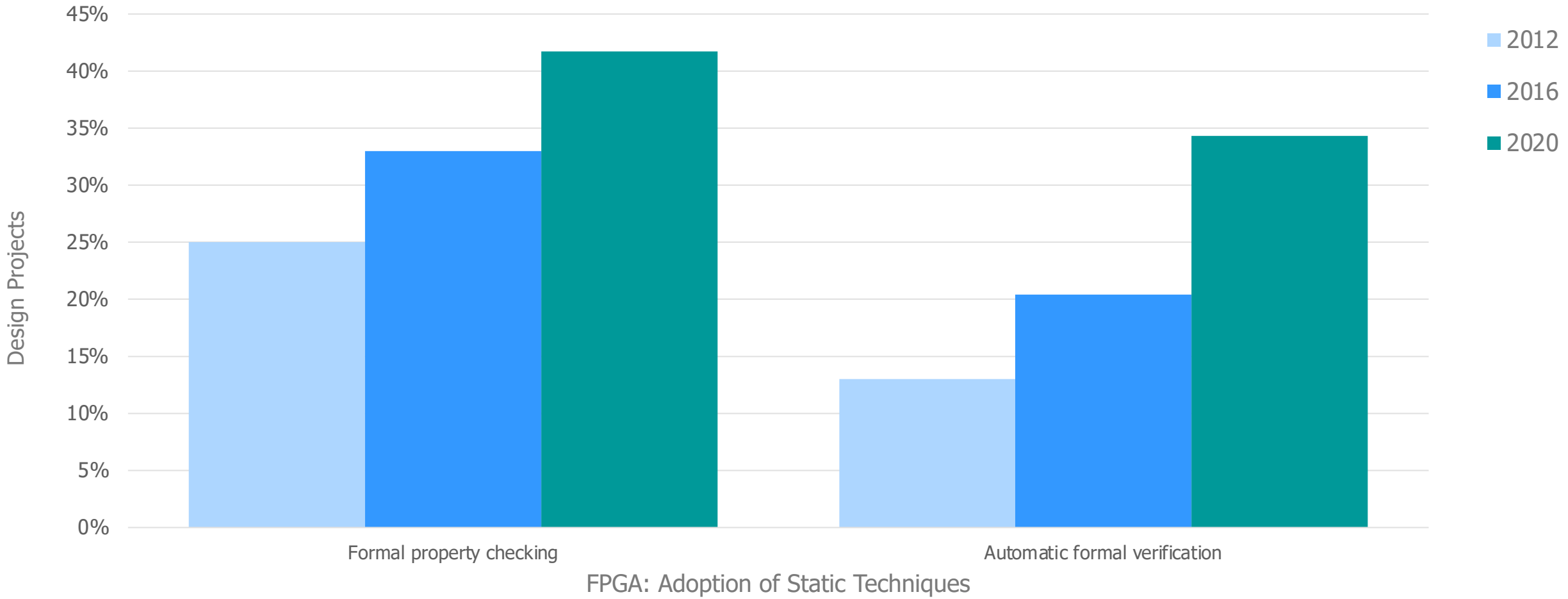
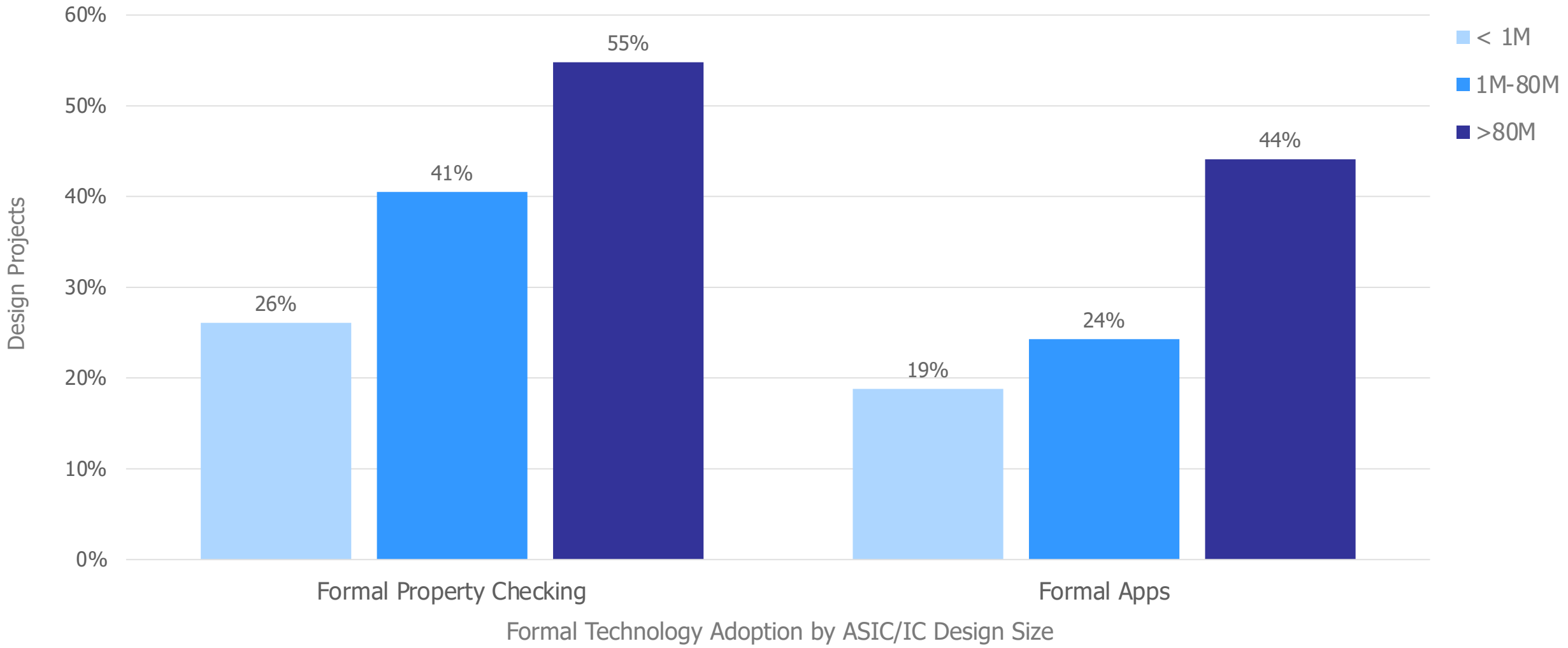
VERIFICATION TECHNIQUES

ASIC/IC Adoption of Formal Technology



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

Formal Technology Adoption by ASIC/IC Design Size



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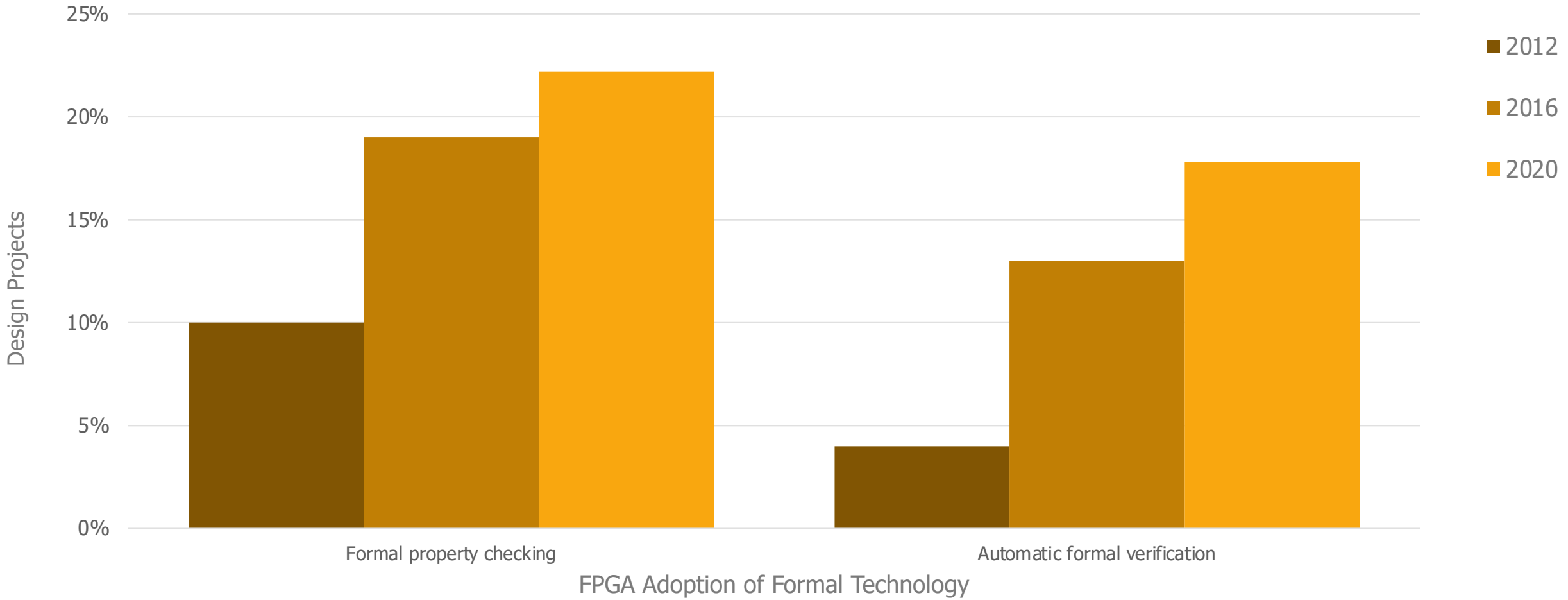
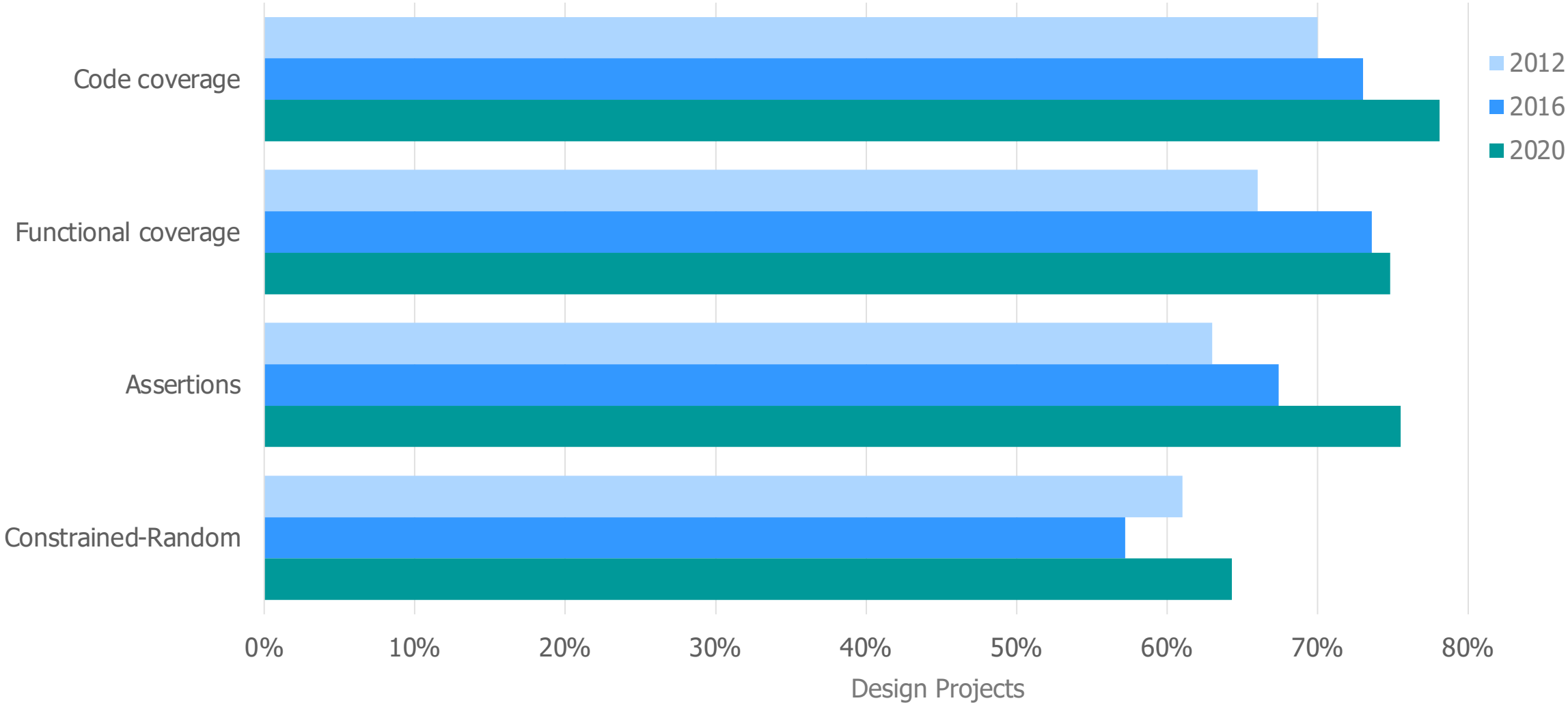
FPGA Adoption of Formal Technology



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

ASIC Adoption of Dynamic Techniques



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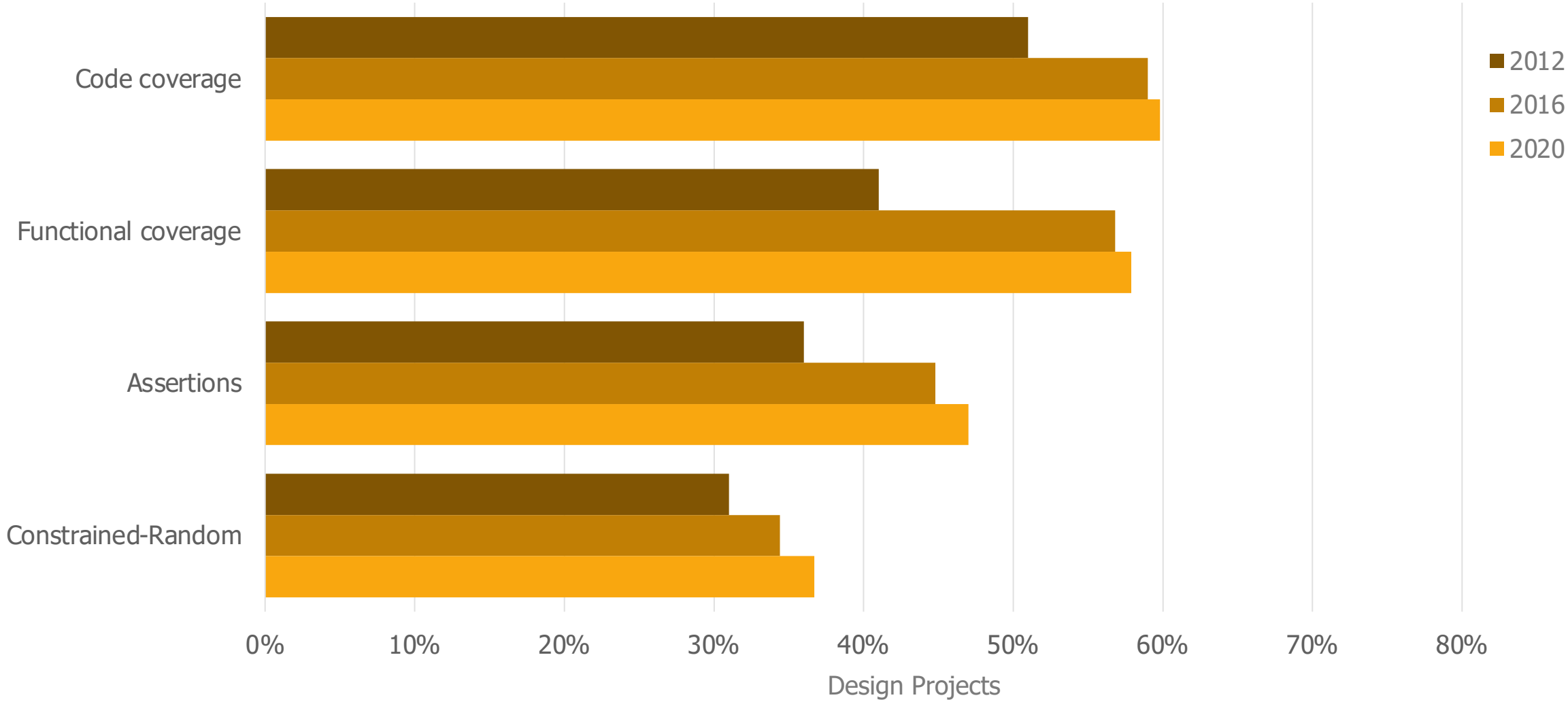
FPGA Adoption of Dynamic Techniques



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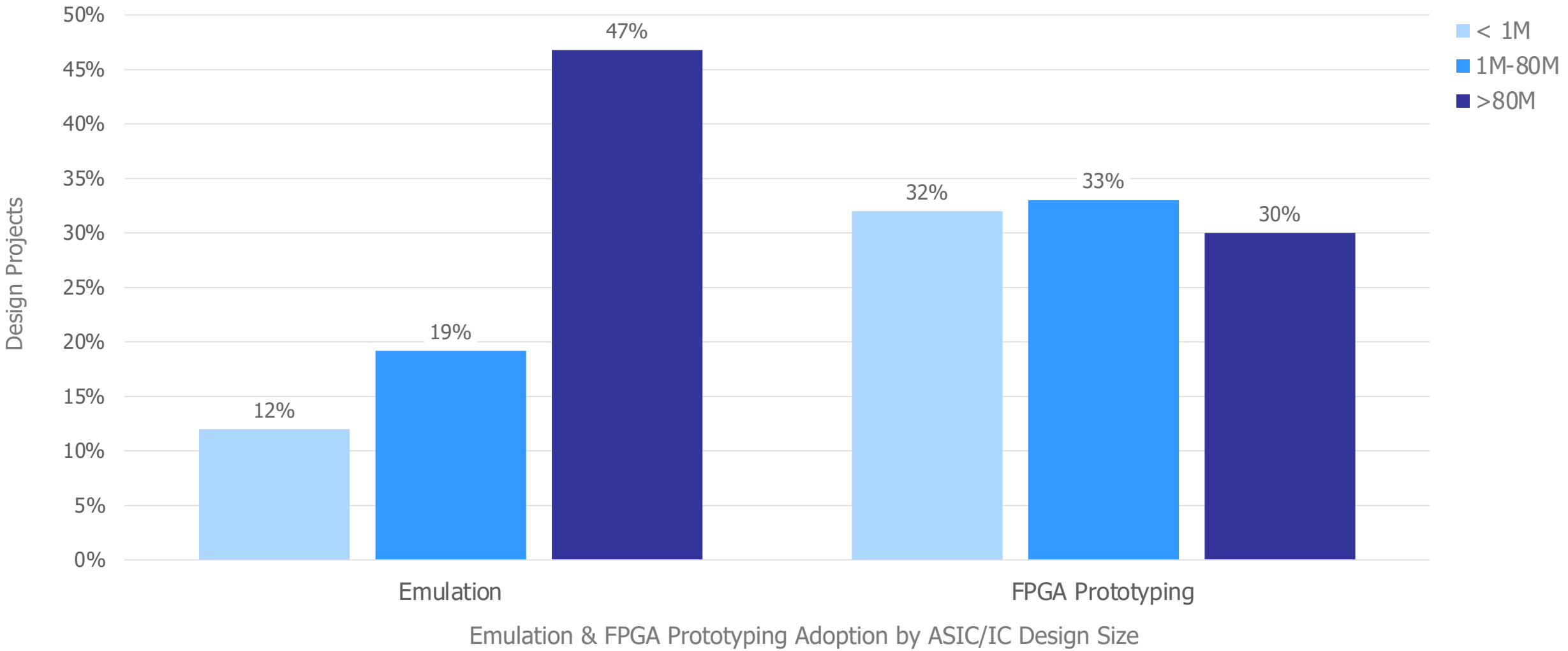
Emulation & FPGA Prototyping Adoption by Design Size



Emulation & FPGA Prototyping Adoption by ASIC/IC Design Size

Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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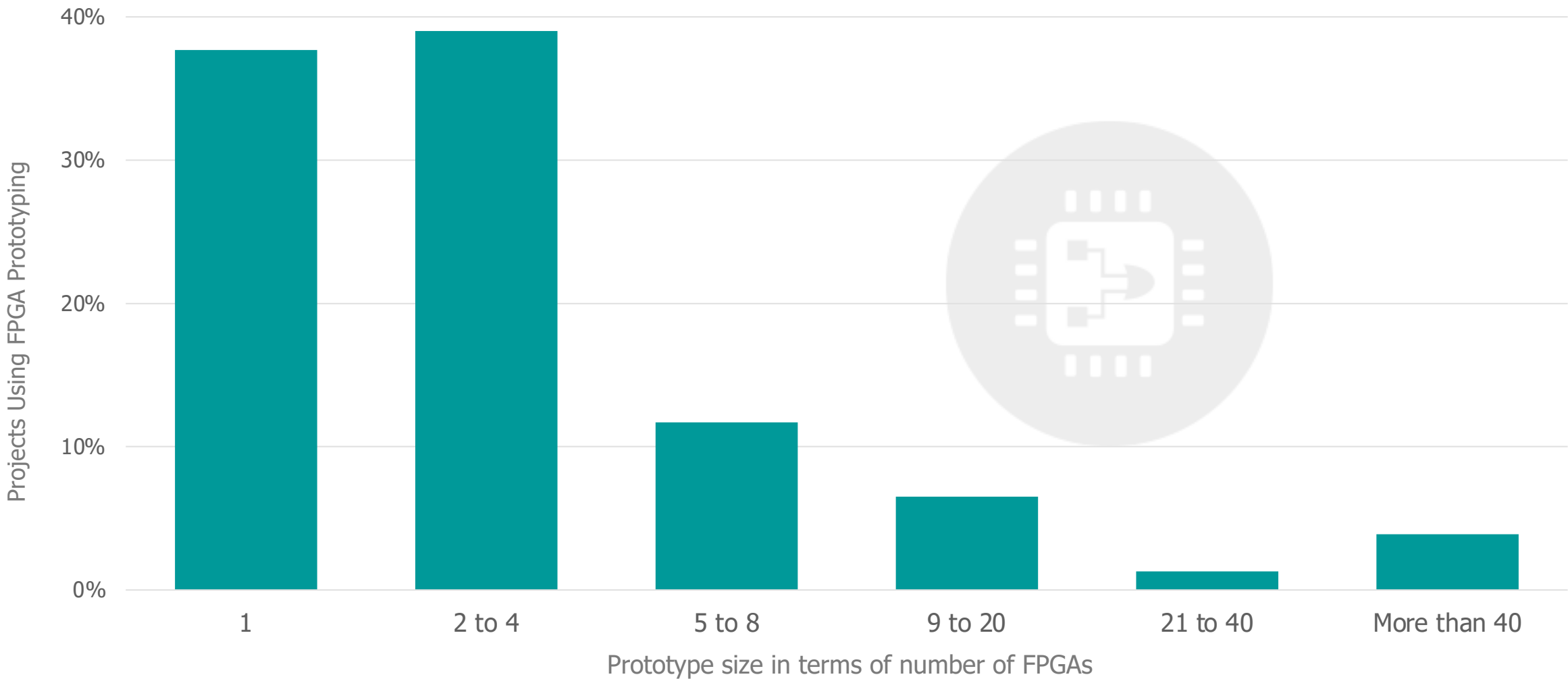
Prototype Size in Terms of Number of FPGAs



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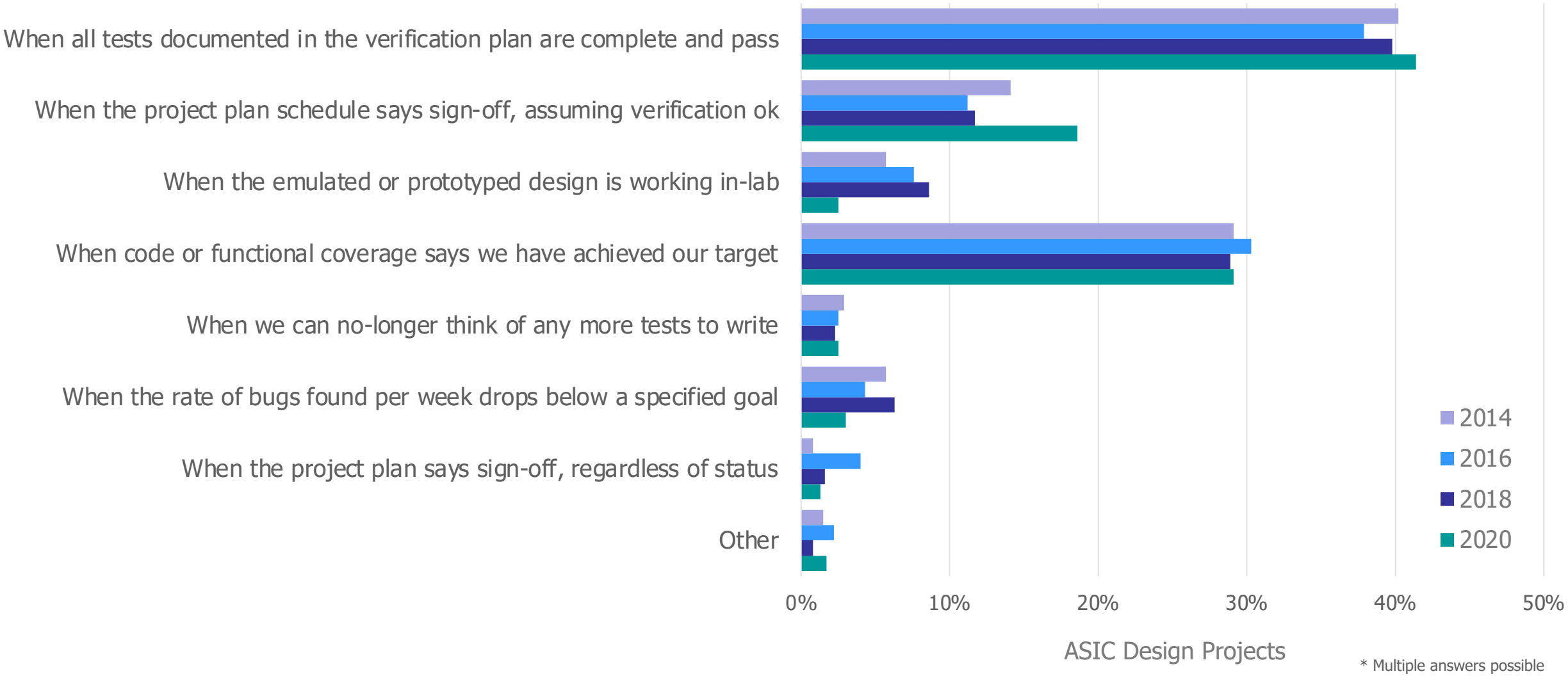
ASIC Signoff Criteria



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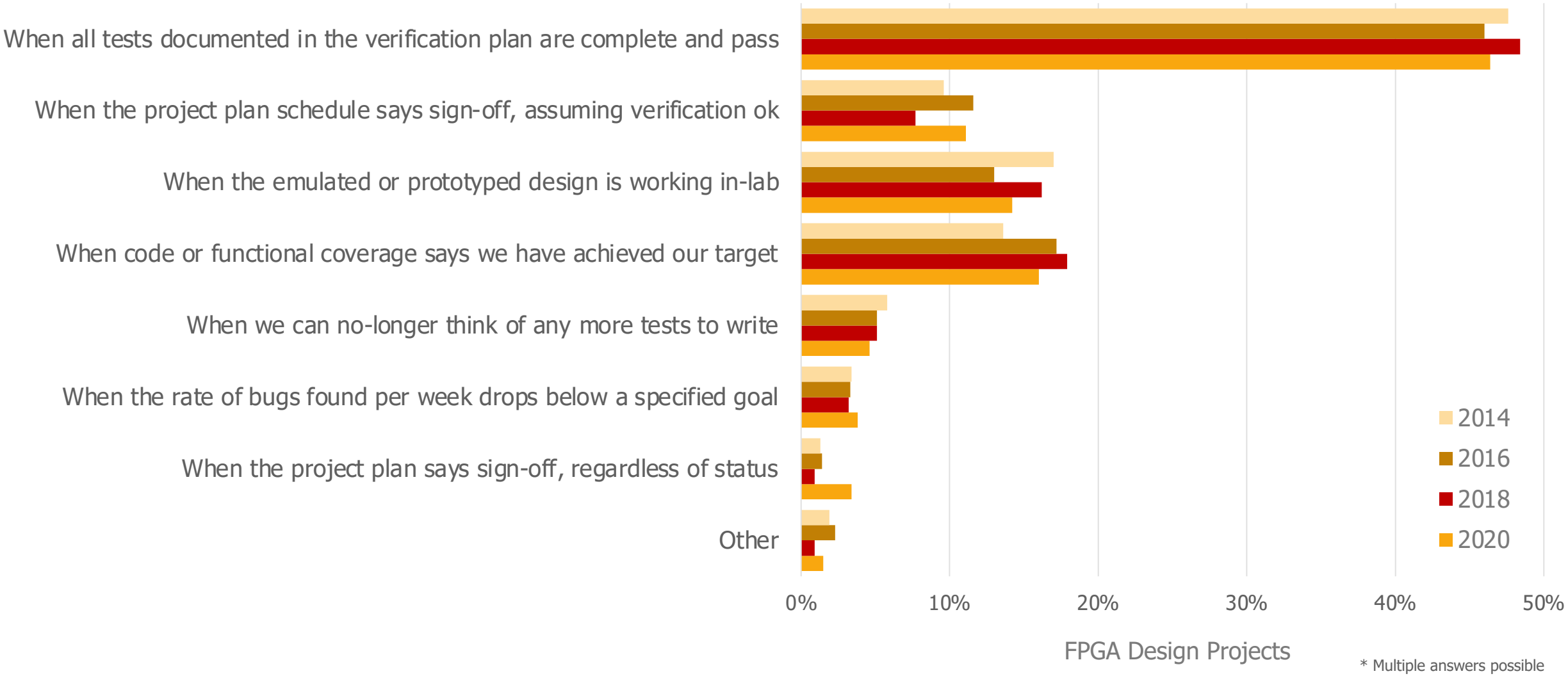
FPGA Signoff Criteria



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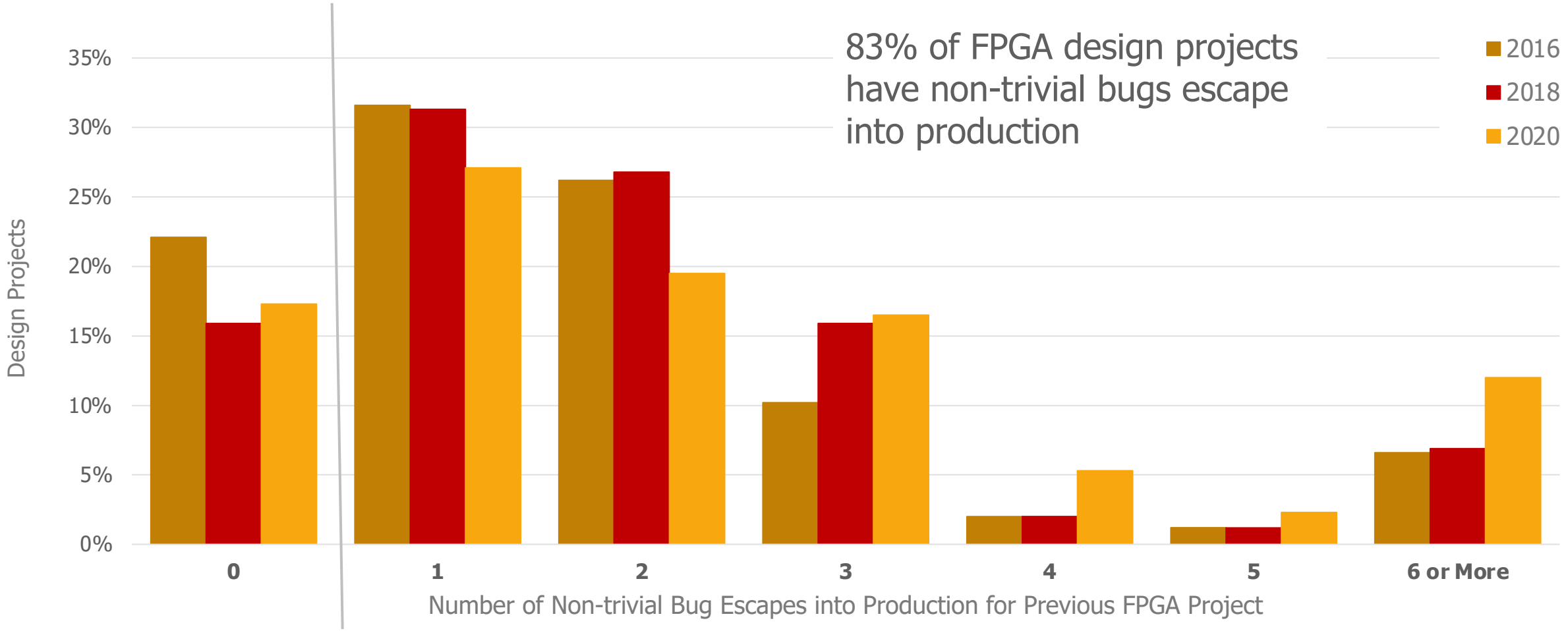
DOES THIS STUFF REALLY WORK?

Number of Non-trivial FPGA Bug Escapes into Production



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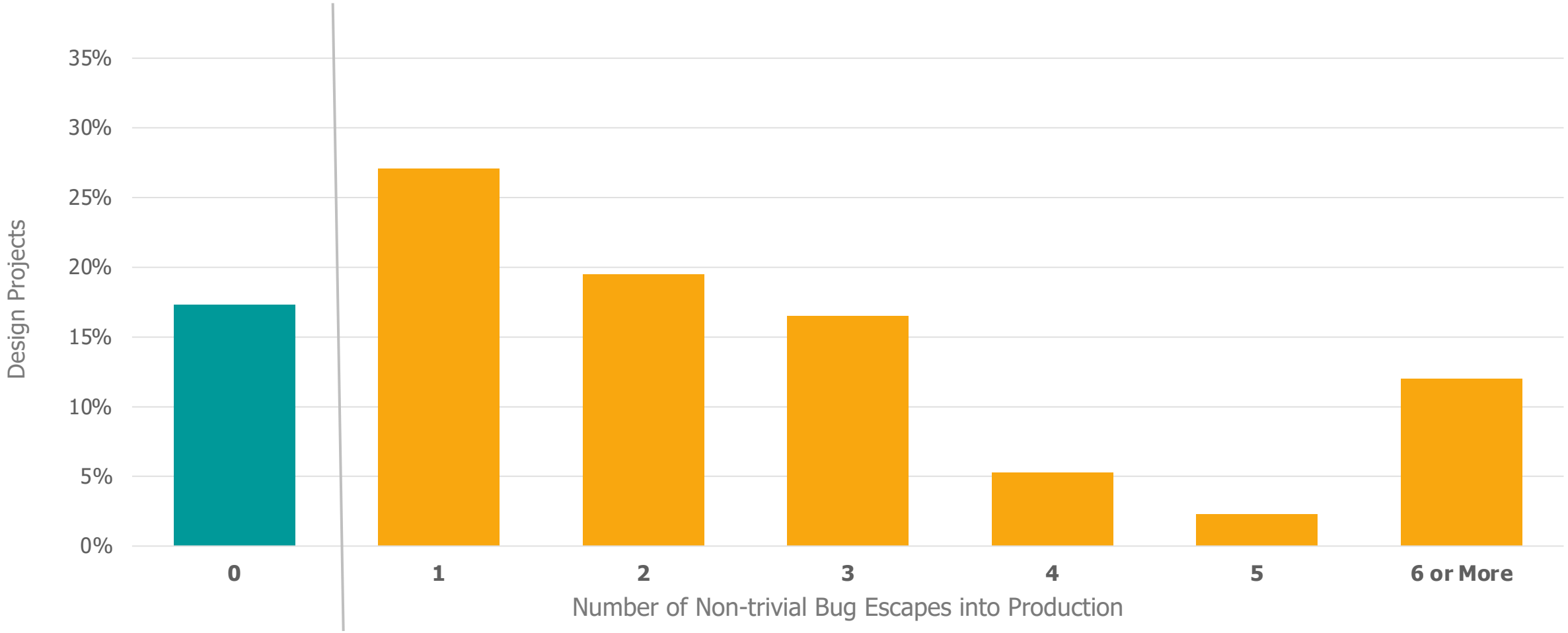
Number of Non-trivial FPGA Bug Escapes into Production



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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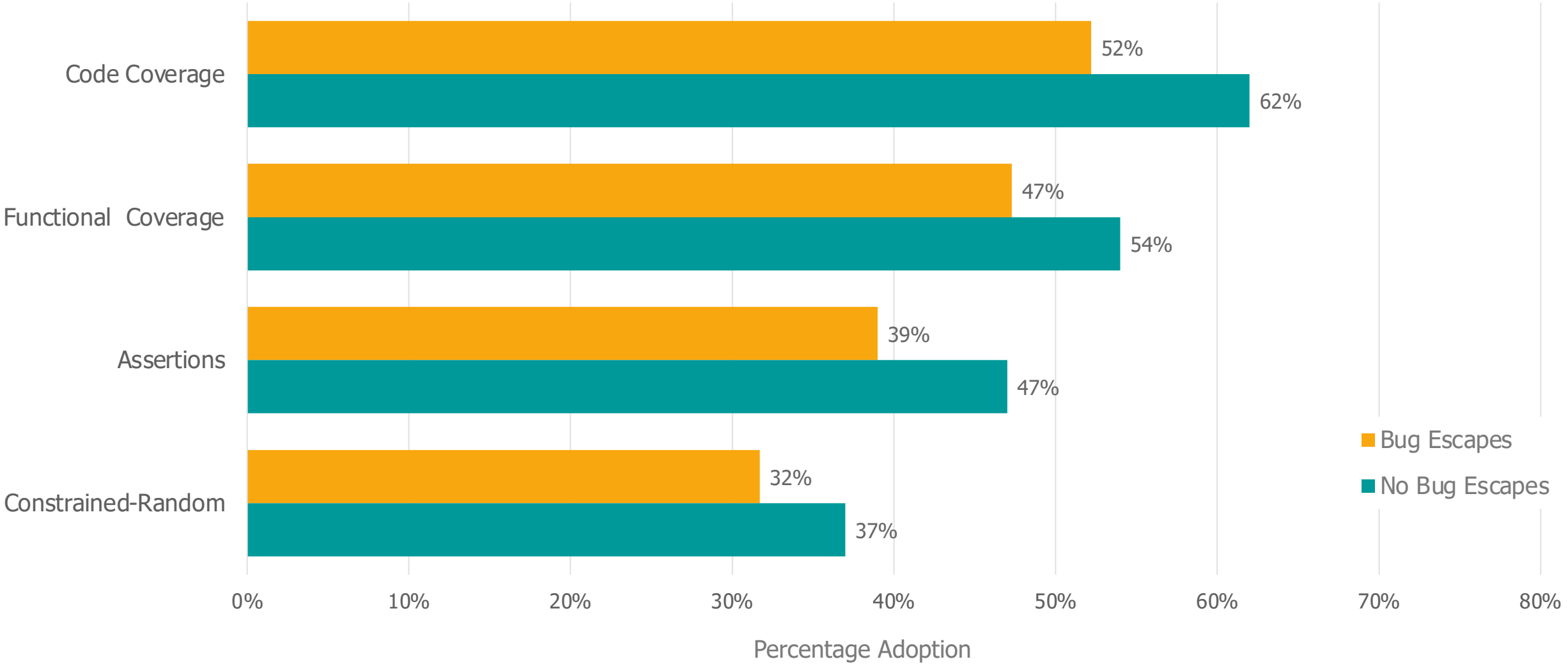
2020 FPGA Verification Technique Adoption and Bug Escapes



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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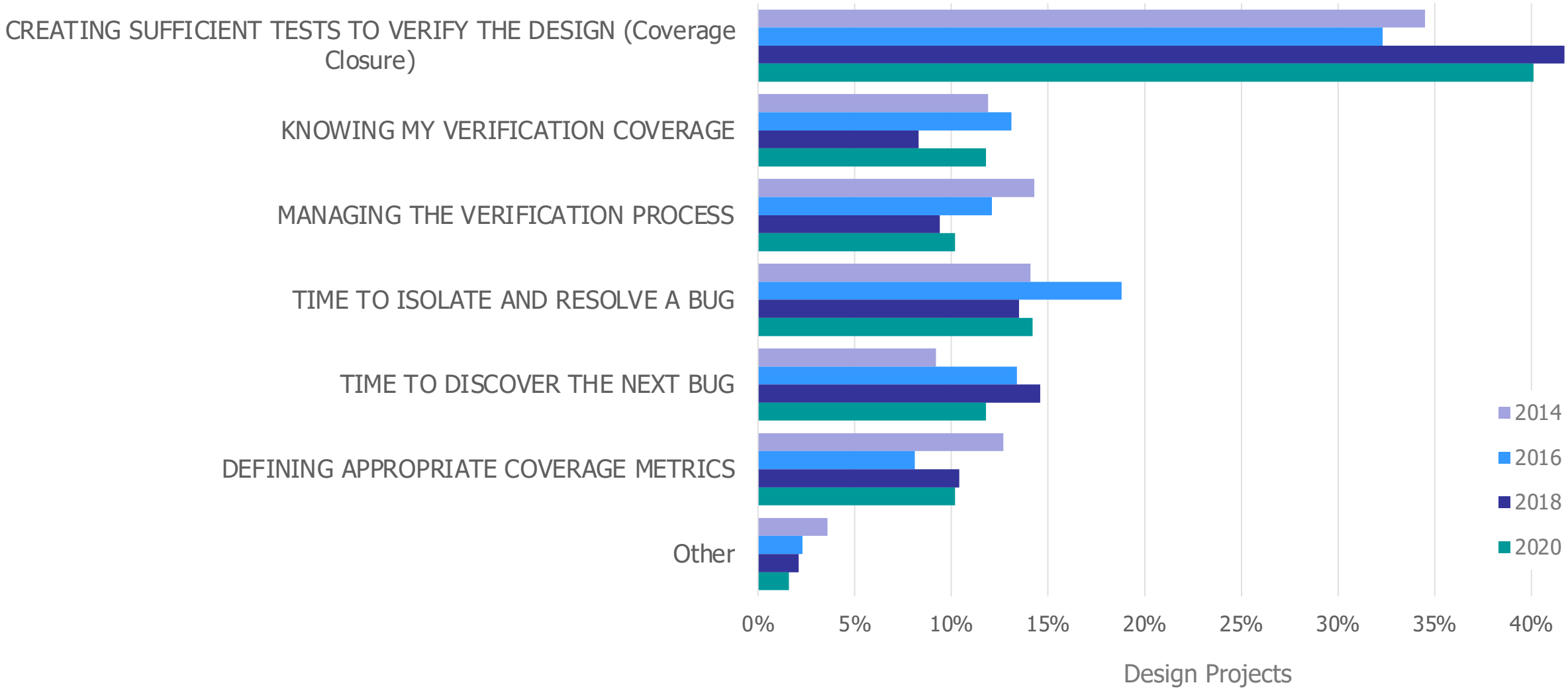
BIGGEST CHALLENGES

ASIC Biggest Functional Verification Challenge



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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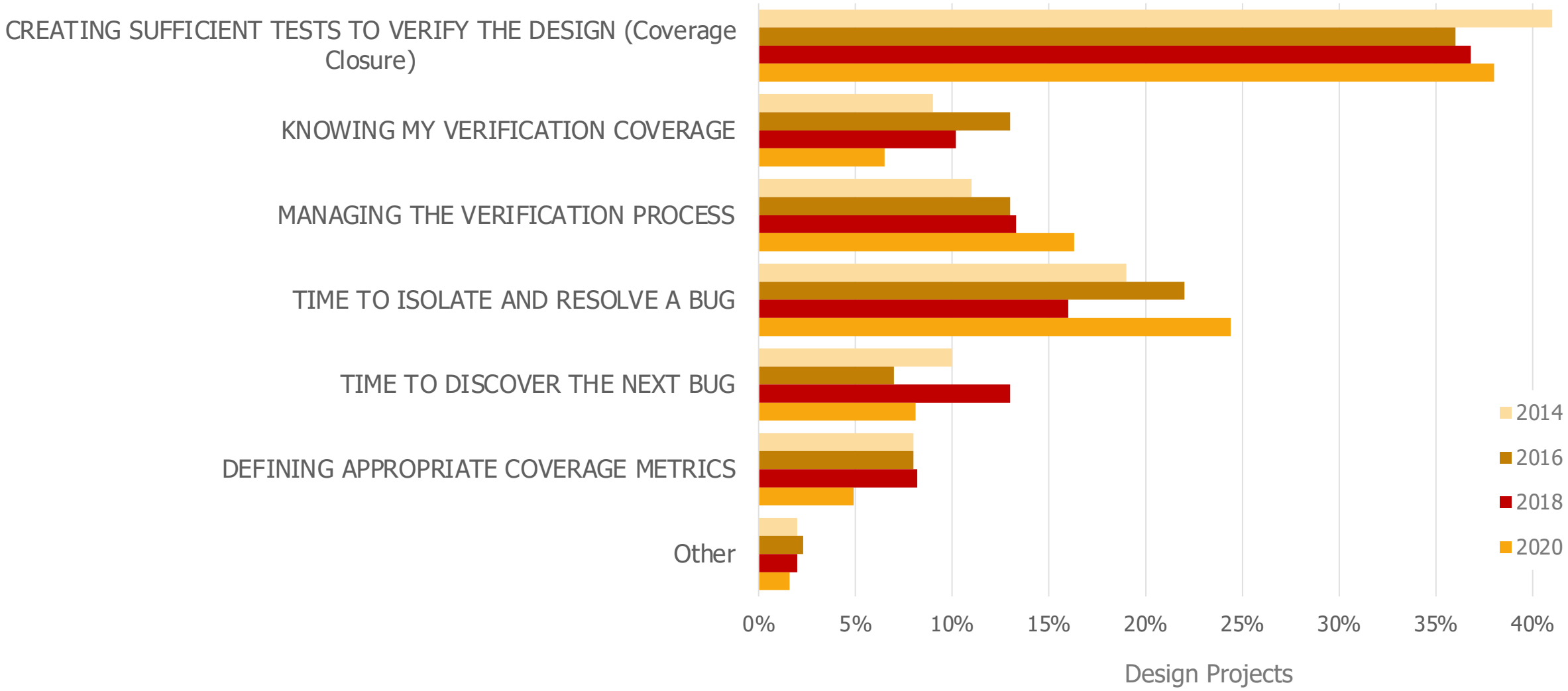
FPGA Biggest Functional Verification Challenge



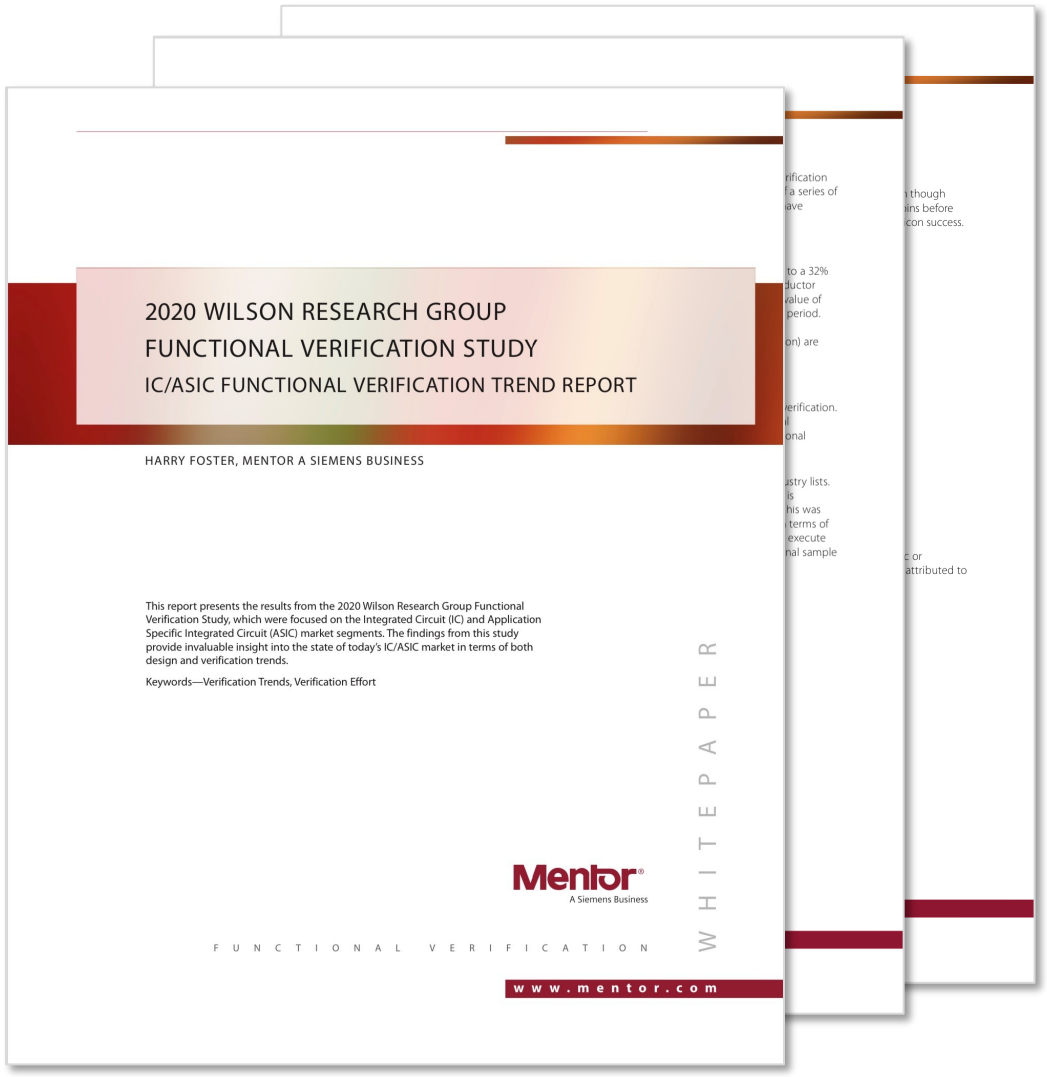
Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

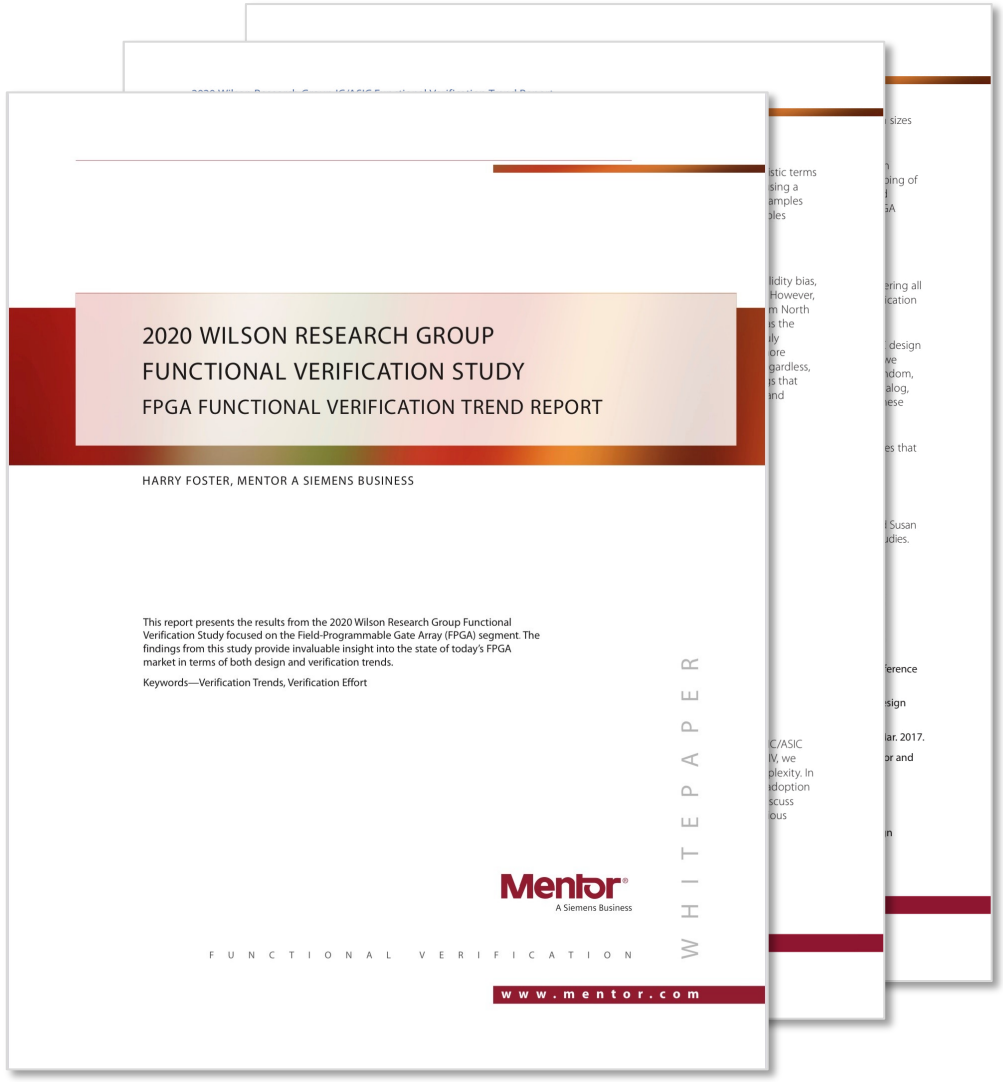
SUMMARY

Summary

- Increased requirements driving complexity
- IC/ASIC projects mature in their processes
- FPGA projects are being forced to mature their processes
- Fewer bug escapes occur in project's with mature verification processes

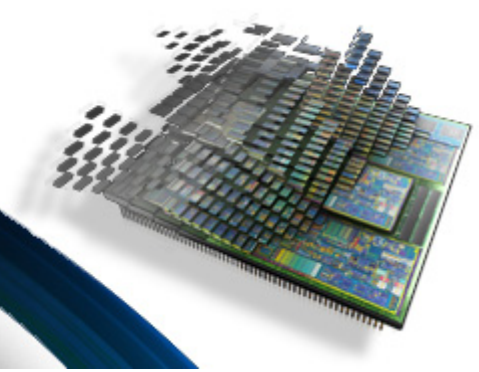
2020 Functional Verification Reports





Verification Academy

The most comprehensive resource for verification training



Industry Data and Surveys

Every two years, Mentor Graphics commissions Wilson Research Group to conduct a broad, vendor-independent survey of design verification practices around the world. Results of the functional verification study demonstrate an ongoing convergence of design and verification practices toward a common methodology.

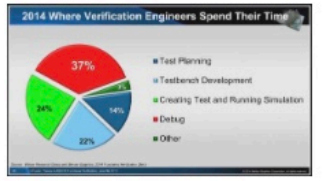
Harry Foster | Acceleration | FPGA Verification | Planning, Measurement and Analysis | Walk

Sessions

Functional Verification Study - 2018

Harry Foster highlights the key findings from the 2018 Wilson Research Group Functional Verification Study, and provides his interpretation and analysis behind today's emerging trends.

ASIC/IC Trends in Functional Verification - 2014

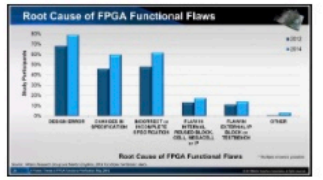


Harry Foster discusses the ASIC/IC verification trends from the 2014 Wilson Research Group Functional Verification Study, and provides some insight into its findings.

Functional Verification Study - 2016

Harry Foster discusses the results from the 2016 Wilson Research Group Functional Verification Study, and provides some insight into its findings.

FPGA Trends in Functional Verification - 2014



Harry Foster discusses the FPGA verification trends from the 2014 Wilson Research Group Functional Verification Study, and provides some insight into its findings.

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