WHY THE DESIGN PRODUCTIVITY GAP NEVER HAPPENED

(Invited Designer Track Paper)

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ABSTRACT

In 1997, SEMATECH set off an alarm in the industry when it warned that productivity gains related to IC manufacturing capabilities (which increased at about 40% per year) outpaced the productivity gains in IC design capabilities (which increased at about 20% per year). In spite of this alarming gap between growing silicon capacity and design capabilities, the industry never felt the effects. Why? This invited talk reviews the findings from the 2012 Wilson Research Group Functional Verification Study and identifies the trends that prevented the design productivity gap. However, a more ominous challenge than the design productivity gap is emerging. While silicon capacity grows at a Moore's Law rate, verification effort grows at a double exponential rate, and the solutions used to close the design productivity gap will not be sufficient to close the verification productivity gap. This invited talk concludes with a discussion on the changes needed to overcome the verification productivity gap.

Index Terms— functional verification

1. INTRODUCTION

In 2002 and 2004, Ron Collett International, Inc. conducted its well known ASIC/IC functional verification studies, which provided invaluable insight into the electronic industry's state and trends in design and verification at those points in time. [1][2] However, after the 2004 study, no other industry studies were conducted—which left a void for those interested in indentifying industry trends.

To address this dearth of information, Mentor Graphics commissioned Far West Research in 2007 [3] and Wilson Research Group in 2010 to conduct new industry studies on functional verification. To avoid influencing the results, both studies were executed as blind studies. This means that the survey participants did not know that the study was commissioned by Mentor Graphics. In addition, to support trend analysis on the data, the survey strictly followed the same format and questions that were asked in the 2002 and 2004 Collett studies.

In the fall of 2012, Mentor Graphics commissioned Wilson Research Group to conduct a new functional verification study. [4] This study was also a blind study, and it follows the same format as the Collett, Far West Research, and previous Wilson Research Group studies. The 2012 Wilson Research Group study is one of the largest blind functional verification studies ever conducted with 616 participants. It is about 3.9 times larger than the original Collett studies, and twice as large as the Far West Research study. Unlike the previous Collett and Far West Research studies that were conducted in North America only, the 2010 and 2012 Wilson Research Group studies are worldwide studies. The regions targeted are:

- North America: Canada, United States
- Europe/Israel: Finland, France, Germany, Israel, Italy, Sweden, UK
- Asia (minus India): China, Korea, Japan, Taiwan
- India

Another difference between the Wilson Research Group studies and all the previous studies is that they both included FPGA engineers. The survey results are compiled both with the combined FPGA and IC/ASIC data (when appropriate) and separately for analysis. Because of space limitations, this paper focuses only on the IC/ASIC results.

Figure 1 shows the percentage makeup of survey participants by the company type. The red bars represent the FPGA participants while the green bars represent the non-FPGA (that is, IC/ASIC) participants.

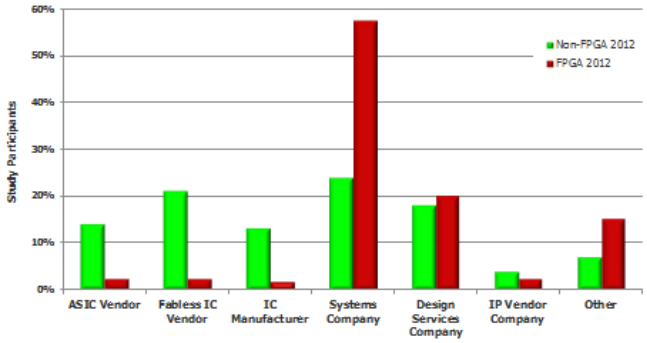

Figure 1. Survey participants' company description

Figure 2 shows the percentage makeup of survey participants by their job description.

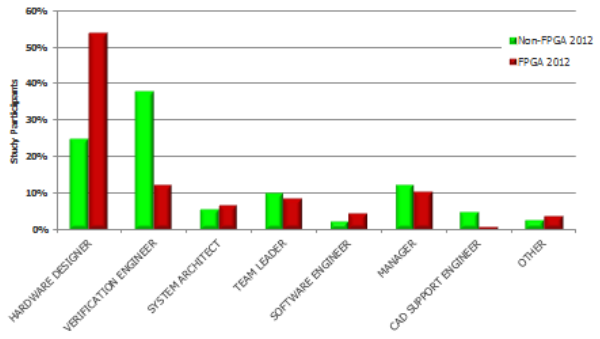

Figure 2. Survey participants' job title description

This invited talk presents the results from the 2012 Wilson Research Group study with some analysis, comments, and obviously, opinions. A few interesting observations emerged from the study:

1. Reuse adoption is increasing.
2. The effort spent on verification is increasing.
3. The industry is adopting more advanced functional verification techniques.

The following extended abstract discusses a few key aspect of the 2012 Wilson Research Group study.

2. EFFORT SPENT ON VERIFICATION

It seems that there is not a single technical functional verification paper published that does not start with the phrase: "70 percent of a project's effort is spent in verification…." Yet, where did this number originate? There has never been a reliable reference to the source of this number, and certainly no credible studies can back up this claim.

In reality, there is no simple answer to the question, "How much effort was spent on verification in your last project?" In fact, it is necessary to look at multiple data points derived from multiple questions to truly get a sense of the effort spent in verification.

2.1. Total project time spent in verification

To try to assess the effort spent in verification, begin by looking at one data point, which is the total project time spent in verification. Figure 3 shows the trends in total project time spent in verification by comparing the 2007 Far West Research study (in gray) and the 2012 Wilson Research Group study (in green).

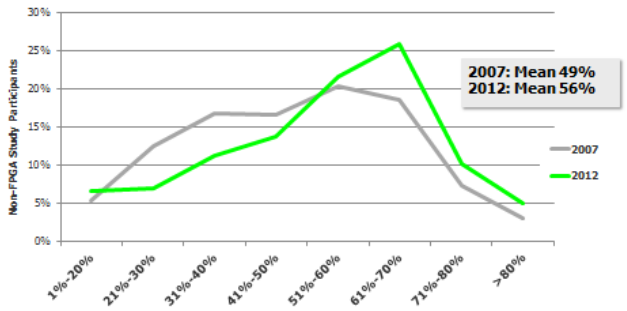

Figure 3. Percentage of total project time spent in functional verification

Notice that in 2007, the mean total project time spent in functional verification was calculated to be 49 percent, and increased to 56 percent by 2012.

2.2. Peak number of verification and design engineers

Next, look at the peak number of verification and design engineers on a project. Figure 4 compares the peak number of IC/ASIC verification and design engineers involved on a typical design project between 2007, 2010, and 2012.

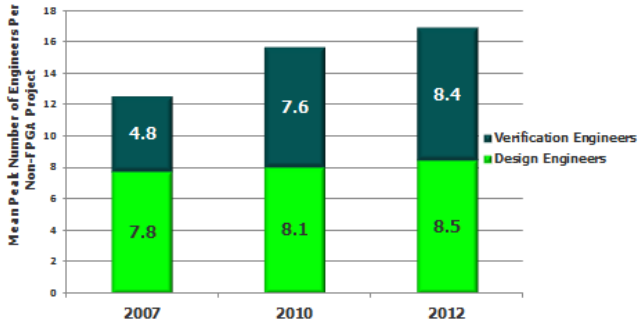

Figure 4. Mean peak number of verification and design engineers

The mean peak number of IC/ASIC design engineers' compounded annual growth rate (CAGR) between 2007 and 2012 is 2.7 percent. However, the mean peak number of verification engineers' CAGR during the same period is 13.1 percent. In fact, today we see about a one-to-one ratio in the number of IC/ASIC verification engineers to design engineers involved on an average project.

2.2. Where engineers spend their time

Design engineers do not spend all of their time only doing design. Certainly, one finding from the Wilson Research Group study is that the mean time a design engineer spends on verification has increased from an average of 46 percent in 2007 to 53 percent in 2013, as shown in Figure 5.

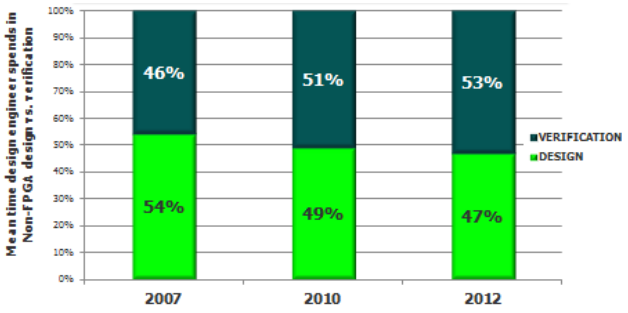

Figure 5. Where design engineers spend their time

Today, we see that design engineers spend more of their time involved with some aspect of verification than they actually spend creating designs. Examples of the designers' involvement in verification range from:

- Small sandbox testing to explore various aspects of the implementation
- Full functional testing of IP blocks and SoC integration
- Debugging verification problems identified by a separate verification team

The Wilson Research Group Study also looked at the mean time that verification engineers spend performing various tasks, as shown in Figure 6. The data indicates that verification engineers tend to spend most of their time involved in debugging. Unfortunately, even with the same project team, the time spent in debugging can vary significantly from project-to-project. This presents scheduling challenges for many managers during a new project's verification planning process. Obviously, to improve predictability and productivity, debugging needs be considered an important area of research, and methodologies and processes that improve debugging times need to be adopted in the industry.

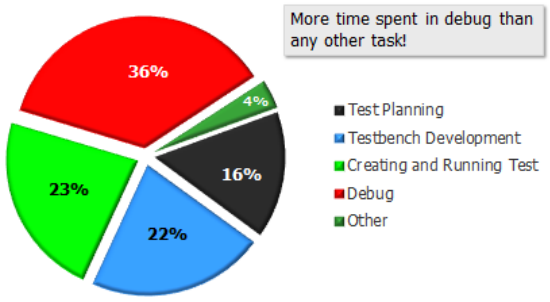

Figure 6. Where verification engineers spend their time

3. VERIFICATION RESULTS

Obviously, a significant amount of effort is being applied to functional verification. An important question the various studies have tried to answer is whether this increasing effort is paying off.

Figure 7 presents the design completion time compared to the project's original schedule. What is interesting is that we really have not seen a change in this trend in over five years. That is, 67 percent of all projects are behind schedule with respect to their original plan. One could argue that designs have increased in complexity in terms of gate counts, embedded processors, and lots of software between 2007 and 2012. Yet, achieving project schedules has not worsened.

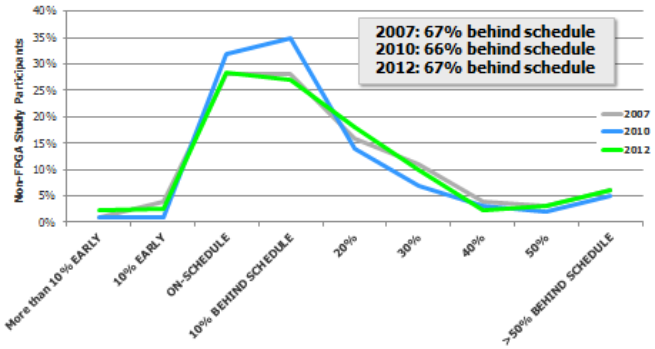

Figure 7. IC/ASIC actual schedule vs. original plan

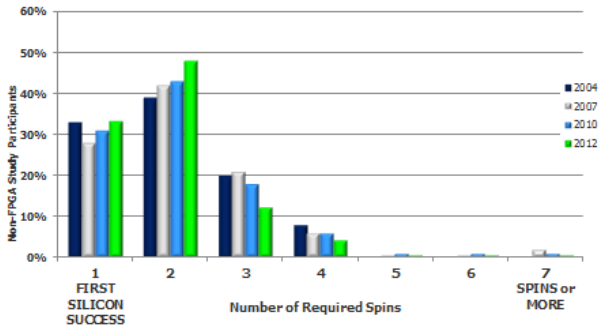

Figure 8. Number of required design spins

Other verification data points worth looking at relate to the number of spins required between the start of a project and final production. Figure 8 shows this industry trend all the way back to the 2004 Collett study. Again, even though designs have increased in complexity, the data suggest that projects are not getting any worse in terms of reducing the required number of spins before production. If anything, there appears to be a slight improvement recently in this trend in projects requiring three or more spins.

4. PRODUCTIVITY GAP

In 1997, SEMATECH set off an alarm in the industry when it warned that productivity gains related to IC manufacturing capabilities (which increased at about 40% per year)

outpaced the productivity gains in IC design capabilities (which increased at about 20% per year). This concern was reiterated by the ITRS in 1999 [5]. Figure 9 illustrates this concept in terms of increasing silicon capacity and improved design capabilities.

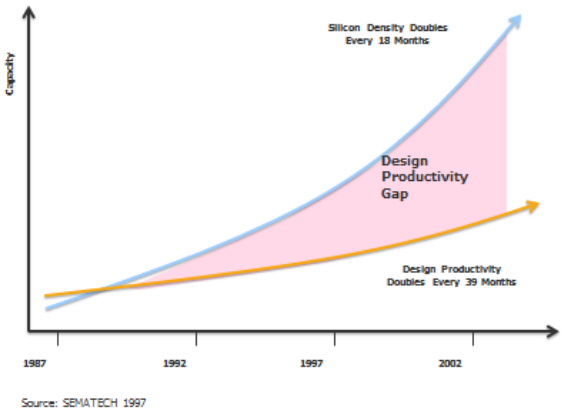

Figure 9. Design productivity gap

In spite of this alarming gap between growing silicon capacity and design capabilities, the Wilson Research Group studies suggest that the industry never felt the effects. For example, in Figure 4 we saw about a five percent increase in the required number of design engineers on a project between 2010 and 2012. Ye, designs continued to increase at a Moore's Law rate during this same period, and the Wilson Research Group study found that projects continued to move to designs with smaller feature sizes as time progressed.

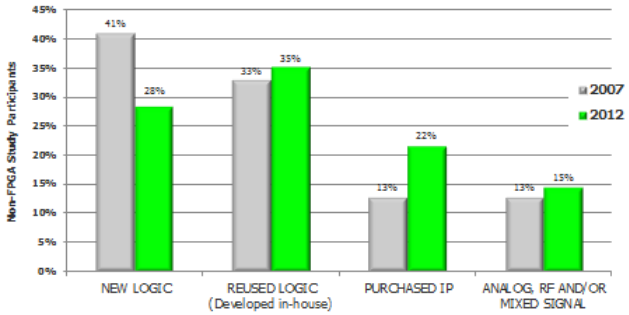

Figure 10. Design composition trends

One of the main contributors to closing the productivity gap has been the emergence of industry internal and external bus standards, which have facilitated the emergence of an IP reuse strategy. Figure 10 shows the mean industry trends in terms of IP reuse. Here you can see that the creation of new logic (e.g., RTL or gates) has decreased by about 32 percent within the last five years, while reused in-house design IP and externally purchased design IP has increased.

However, a more ominous challenge than the design productivity gap is emerging. While silicon capacity grows at a Moore's Law rate, verification effort grows at a double exponential rate, and we claim that a verification reuse strategy in itself will not be sufficient to close the verification productivity gap. Design reuse practices seem to have contained the growth in demand for design engineers. Our study found that 62 percent of a project's verification environment is currently being reused (either internally develop or externally acquired verification IP). Yet, the demand for verification engineers has increased significantly as shown in Figure 4.

3. CONCLUSION

The 2012 Wilson Research Group study found that the effort spent in verification (as measured by percentage of project time, peak number of engineers, and designer time spent in verification) continues to increase. The study also suggests that verification reuse strategies in themselves will not be sufficient to close the verification gap. History has repeatedly shown that increasing the level of design abstraction improves productivity (in the order of 100 to 1000x), while reducing bug density in code. These improvements combined with verification reuse strategies and newer acceleration techniques will be necessary to close the emerging verification gap. This invited talk introduces a few of these newer acceleration techniques that are not covered in this extended abstract.

The complete set of data from the study is too vast to present in a single paper. Hence, this extended abstract focused on the aspect of verification effort and the productivity gap. More details concerning the study results are available at [4].

4. REFERENCES

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