UK 2011

Bryan Dickman, ARM	**Complexity** • Design for verification	**Scalability** • Meeting our need for cycles	**Completeness** • How do we know when we are done?
Olivier Haller, ST	**Scalability** • Is exhaustive RTL simulation scalable? • Data management	**Complexity** • Nobody understands the full system	**Productivity** • Do more with same budget • Faster with derivatives
Hans Lunden, Ericsson	**TLM in verification** • Improved TTM	**VIP** • Improved quality • Make or buy?	**Design for verification** • Quality and TTM
Clemens Muller, Infineon	**Complexity** • Mastering the verif complexity	**Debug Automation** • Managing all the data	**Requirements driven verification**

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Our Top3 Verification Challenges

- **Top1: Mastering Verification Complexity**
  - Continuous increase in number of IP's and embedded processors
    - 2006: 30-40 IP's, 1 CPU
    - 2011: 80+ IP's, 6+ CPU's
    - *2016: 120+ IP's, 20 CPU's ?*
  - The more IP's the higher the risk of late spec & implementation changes
  - Driving towards true Hw/Sw Co-Verification
  - Reuse of verification environments / stimulus from IP-level into big multi-CPU SoC environments

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2. Scalability

- **Constrained-random simulation has been proven as a good bug-hunting flow, but...**
  - How much simulation will be enough for a 10 GHz CPU?
  - How many cycles to verify 2 weeks at target speed of 1GHz?
    - Answer: 0.6 x 10^{15}

	Simulation (KHz)	Emulation (1 MHz)	FPGA (10 MHz)	Si (1 GHz)
Target cycles 10^{15}	1,000,000 sim slots	1000 emulation slots	100 FPGA slots	1 chip
Achievable cycles	10^{11}	10^{12}	10^{14}	10^{15}

- ***How will we scale simulation, emulation, FPGA to next gen of CPUs?***
- ***What are the alternatives?***

UK 2012

Geoff Barrett, Broadcom	**Scalability** • At chip level	**Verification resources** • Too much on diversions	**EDA Tool Maturity**
Andre Winkelmann, Wolfson	**Requirements Tracing**	**Scalability** • Ease of verifying derivatives	**Mixed Signal** • The boundaries are fading
Andrew Bond, NVidia	**H/SW Co-verification** • SW engineers avail to write real SW	**Performance Verif** • Everybody finds own solution	**Resources** • Shortage of verif engineers
Steve Holloway, Dialog	**Verification Completion** • Increasingly hard	**Achieving Reuse**	**Mixed Signal** • MDV for AMS
Tim Blackmore, Infineon	**Complexity** • Reducing verif complexity	**Change** • Making verif more agile	**Better use of sim cycles** • How to improve use of cycles?

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Recruitment

- **Verification engineers are always in demand**
- **Even with some industry-wide unification of methodologies finding good engineers doesn't seem to be getting easier**
- **With more design re-use and verification outsourcing flexible engineers seem harder to find**

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Challenge 3 – Mixed Signal

- **MS verification made easy**
  - How do analogue and digital engineers work together?
  - Multitude of skills required
- **Boundary is fading**
  - Analogue verification incorporates digital techniques
  - Digital verification incorporates analogue features
- **Variety of modelling techniques and abstractions**
- **Power aware mixed signal verification**
- **UVM-AMS adoption**

France 2012

Laurent Arditi, ARM	**Bug Avoidance** • Functionally correct designs?	**Bug Hunting** • Improved hunting & completion	**Bug Absence** • Proving absence of bugs
Thomas Goust, ST-E	**Design Complexity**	**IC to chipset** • Multiple ICs	**Leading-Edge Tech** • Outsourcing
Jerome Bombal, TI	**HW-SW Co-Verification**	**Fast platform prototyping**	**Real-world functional coverage**
Christophe Chevallaz, ST	**Verification Reuse** • Lots of opportunity	**System Verification**	**Verification Mgt** • Data mgt

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Challenge 3 – Verification Management

- **The challenge to manage huge amount of verification data**
  - Amount of verification data make more complex the risk decision of verification closure
- **Some Directions partially or to be implemented**
  - Refine the verification Metrics
  - Merge the metrics (SOC / IPS – various source)
  - Usage of MySQL data Base
  - Leverage on Business Intelligence tool to support Verification Closure
  - Define metrics on non-functional properties (performance, power, energy, temperature, …)

Germany 2012

Martin Ruhwandl, Lantiq	Multi-Language Verif environments	Debugging • More automation	3rd Party IP integration • And VIP
Michael Rohleder, Freescale	Synthesis/Timing Constraints	Holistic Coverage • Combining views	Disconnected Views • Functional, timing, power, SW
Wolfgang Ecker, Infineon	Requirements driven verification	TopDown/ BottomUp • Verif at right level	Heterogeneous Systems • Digital, Analog, FW

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- **Required by ISO 26262**
  - "Road vehicles – Functional safety" and other similiar standards
- **Validate the verification**
  - Have the right things been verified
  - Avoid that requirements haven't been verified and things have been verified, that haven't been required
- **Reuse implementation of verification goal**
- **Keep track with change requests**
- **Enable impact analysis**

India 2013

Sainath Karlapalem, NXP	AMS Verification	Dynamic Power Verif	Timing Verification
Udaya Kumar Napa, MaxLinear	Coverage Closure	Integrating Levels of Verif	Requirements driven verification
Desikan Srinivasan, ARM	Exploiting Formal	System level coherency	Verif Schedule Predictability

Analysis

Complexity	6
Integrating Languages, Views and Techniques	6
Completeness	5
Productivity	5
Scalability	4
Reuse	4
Requirements Driven Verif	4
System	4
Mixed Signal	3
Debug	2
HW/SW	2
Demonstrating Bug Absence	2
Synthesis/Timing Constraints	2
Performance	1
Resources	1
Change	1
Design for Verif	1
Leading Edge Technology	1
Verification Data Mgt	1
Dynamic Power	1
Predictability	1