

QUIS CUSTODIET IPSOS CUSTODES?
**(WHO WATCHES THE DV ENGINEERS?
THEMSELVES?)**

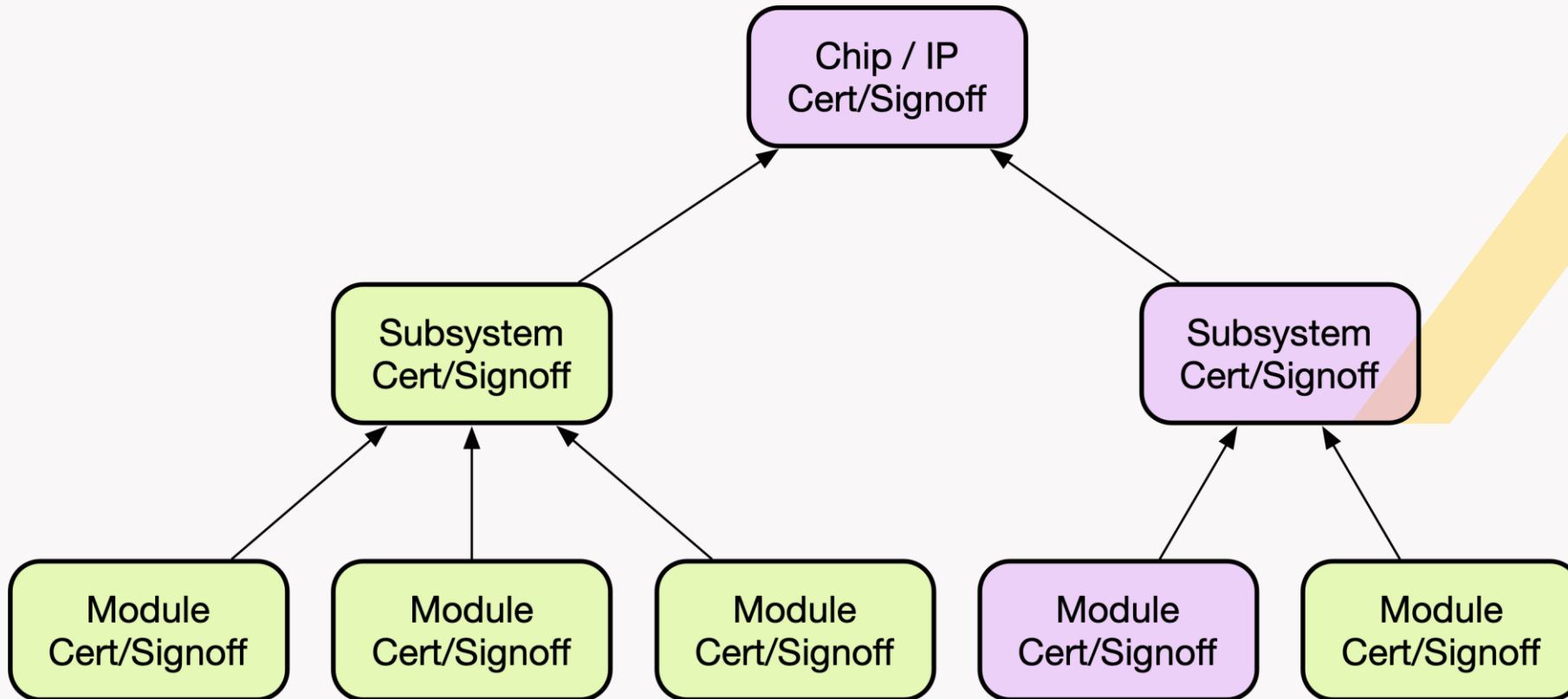


GRAPHCORE

DV PROCESS CERTIFICATES & SIGNOFF REVIEWS



SIGNOFF PYRAMID



ABLE, INEXPERIENCED DV ENGINEERS

Do senior engineers review and understand every line of code?

Certificate / signoff process should be aimed at these engineers



CERTIFICATES

- Checklist
- Guidance
- Reporting – DV eng populate
- Prepare for review



CERTIFICATE EXAMPLE TEMPLATE

Is there 100% Functional Coverage?

Has a GLS regression been run?

(Might need TB mods if probes used)

Has mutation testing been run?

(Not gating)



CERTIFICATE EXAMPLE COMPLETED

Is there 100% Functional Coverage? **Yes**

Has a GLS regression been run?
(Might need TB mods if probes used)

Has mutation testing been run?
(Not gating)

No

Some

Only O/P ports



CERTIFICATES

Not too long but list every important check before shipping (Tricky balance)

‘YES’ answers good (quick review)

Give brief explanation

Maintain certificate template

- Add new checks when you’ve nearly missed issues



SIGNOFF REVIEWS

Review Certificate

Skip 'YES' answers

Discuss others



SIGNOFF CRITERIA



DISCRETION?

Signoff Discretion?

None

Some

Yes

What risk is acceptable?

FUNCTIONAL COVERAGE

Signoff Discretion?

None

Some

Yes

Approved spec – same hierarchy level as DV module

Verif Plan – defines FC

FC must have

FC %age of cross bins hit

- Mission mode vs Debug mode FC holes

STRUCTURAL COVERAGE

Signoff Discretion?

None

Some

Yes

Line / expression / toggle 100%

Holes waived

Waivers reviewed each tapeout



SOAK TESTING

Signoff Discretion?

None

Some

Yes

> 10x number of seeds to find the last bug



TESTS PASSING

Signoff Discretion?

None

Some

Yes

All failure modes must be understood to be TB issues



TOOL WARNINGS

Signoff Discretion?

None

Some

Yes

Review all warnings

Multiple simulators / linters

Warning waiver system? Review waivers



BUG CURVE

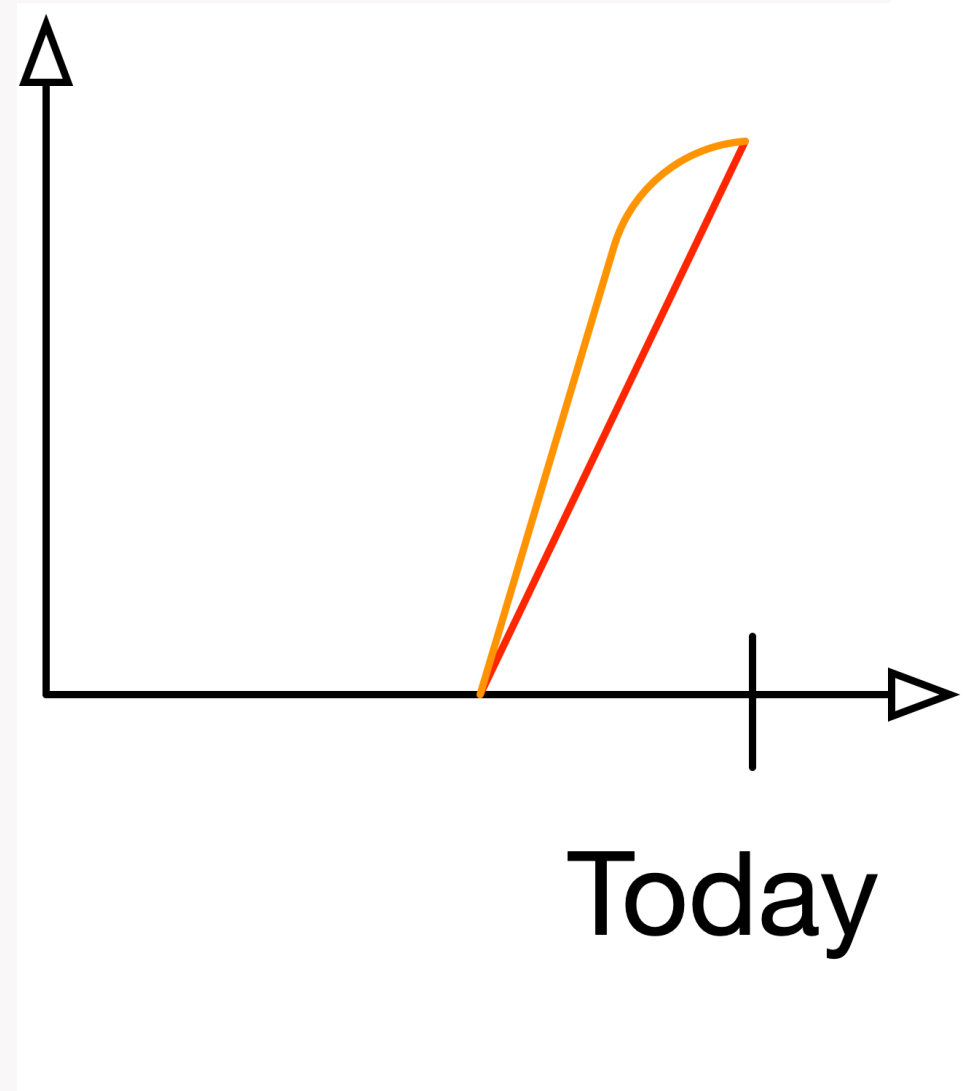
Signoff Discretion?

None

Some

Yes

3 Bugs found and fixed each week for 4 weeks until TO day?



XPROP

Signoff Discretion?

None

Some

Yes

(LRM simulation is X optimistic)

Realistic xprop mode RTL level regression

Gate level sim (but GLS is x pessimistic)

GLS issues when TB probes internals



GLS SDF

Signoff Discretion?

None

Some

Yes

SDF sims are critical check on STA



RTL MUTATION

Signoff Discretion?

None

Some

Yes

Mutated (broken) RTL should fail tests

- Check module output ports
- Random mutations within RTL
- 100% Mutations detected / waived

ETC.

Signoff Discretion?

None

Some

Yes

Many other things, not time for ...

Create and maintain your own Certificate 😊



LEFT SHIFTING SIGNOFF



SIGNOFF IS SLOW

Bureaucratic

Manual process

Only done once per tapeout

On critical path



LEFT SHIFT SIGNOFF – CONTINUOUS DELIVERY

Automate EVERYTHING

Full regression / signoff / delivery continuously
(every week)

Make all reports easily available



THANK YOU

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