Introduction to the **Design Verification Unit** **COMS30026**

(COMS30086)

Kerstin Eder 🎗

Trustworthy Systems Lab

University of BRISTOL

Department of COMPUTER SCIENCE

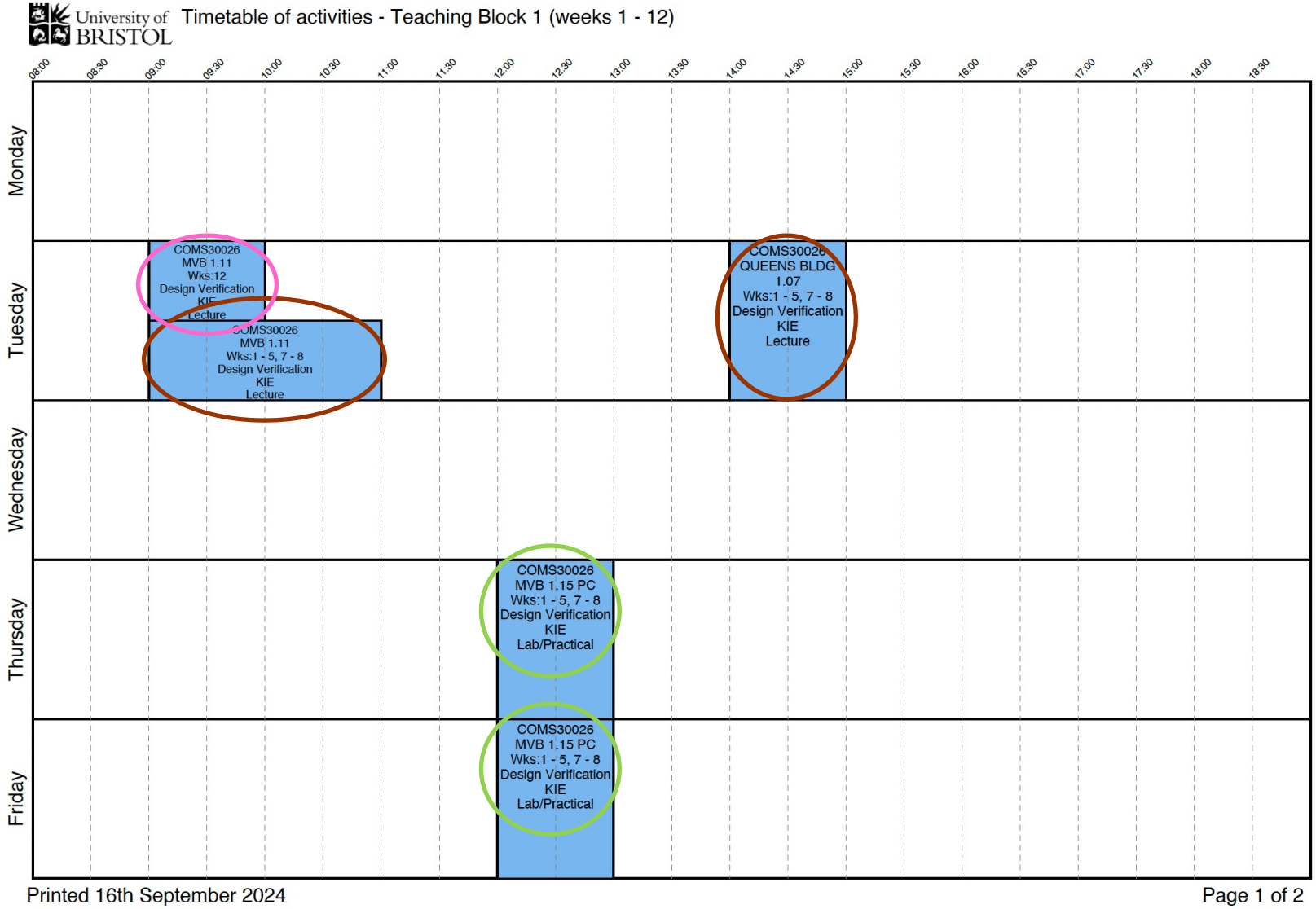
Welcome to Design Verification

- Lecturer and Unit Director
  - Kerstin EDER
  - School of Computer Science
- Lecture slides, exercises and additional material are available at uobdv.github.io/Design-Verification/
- Pre-recordings of all lectures are available on Blackboard
  - Topics for each week can be found on github
- Comments and feedback are always welcome
  - Blackboard “Discussion forum”

Design Verification Unit Details

- Lectures during weeks 1-5, 7-8 and week 12
  - See timetable for lecture times and locations
  - A revision session is scheduled for Week 12

Timetable


University of BRISTOL
Timetable of activities - Teaching Block 1 (weeks 1 - 12)
08:00
08:30
09:00
09:30
10:00
10:30
11:00
11:30
12:00
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15:00
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16:00
16:30
17:00
17:30
18:00
18:30
Monday
Tuesday
Wednesday
Thursday
Friday
COMS30026
MVB 1.11
Wks:12
Design Verification
KIE
Lecture
COMS30026
MVB 1.11
Wks:1 - 5, 7 - 8
Design Verification
KIE
Lecture
COMS30026
QUEENS BLDG
1.07
Wks:1 - 5, 7 - 8
Design Verification
KIE
Lecture
COMS30026
MVB 1.15 PC
Wks:1 - 5, 7 - 8
Design Verification
KIE
Lab/Practical
COMS30026
MVB 1.15 PC
Wks:1 - 5, 7 - 8
Design Verification
KIE
Lab/Practical
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  - Microsoft Teams:

    COMS30026: Design Verification (Teaching Unit)

Please check your timetable regularly in case of any changes.

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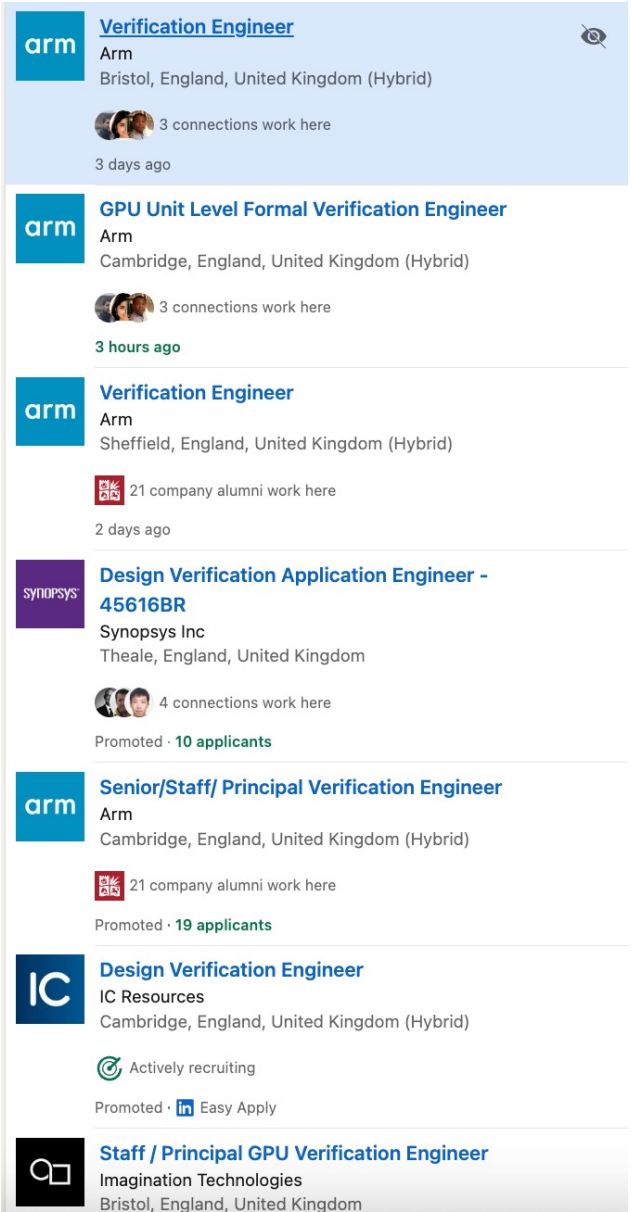
    COMS30026: Design Verification (Teaching Unit)

Please check your timetable regularly in case of any changes.

- Practical Work during weeks 1-5, 7-8 and in weeks 9-11 CW
  - Thursdays 12:00 (50 min) and
  - Fridays 12:00 (50 min) lab sessions
    - MVB 1.15 PC lab
    - Lab support on demand

What is this unit about?

Aim: To familiarise you with the state of the art in Design Verification, and to give you the **technical background** plus some of the **practical skills** expected from a professional Design Verification Engineer.



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Aim: To familiarise you with the state of the art in Design Verification, and to give you the **technical background** plus some of the **practical skills** expected from a professional Design Verification Engineer.

- **Pre-/Co-requisites:** programming experience and a basic understanding of computer architecture

Unit Outline

Lecture Topics

- Introduction: What is Verification? What is a Testbench?
- Verification hierarchy, driving & checking, verification tools
- Verification cycle, methodology and plan
- Simulation-based Verification: stimuli generation, checking, coverage
- Advanced Testbench Design Methodology with SpecMan Elite and e
- Assertion-based Verification (ABV)
- Functional Formal Verification and Property Checking DEMO

Practical work

- Exercise 1: Teach yourself the basics of the Verilog HDL
- Exercise 2: Introduction to the ModelSim/Questa Simulator
- Practical 1, weeks 2-4: Verification of calculator design with ModelSim
- Exercise 3: How to collect Code Coverage with ModelSim/Questa
- Exercise 4: Introduction to SpecMan Elite and e
- Practical 2, weeks 5-8: Advanced testbench design with SpecMan Elite, the e language and formal verification with JasperGold (optional)

Unit Learning Outcomes

On successful completion of this unit, ALL students will be able to:

1. Discuss the process of design verification, its complexities and limits.
2. Describe a variety of state-of-the-art verification techniques, including test-based and formal methods, their foundations, practical use, advantages and limits.
3. Set verification goals, select suitable verification methods and techniques to achieve these and assess the associated risks.

When the unit is taken with the associated 20 credit MAJOR option, students will also be able to:

4. Compile a verification plan, organise resources and perform a functional verification (as part of a small verification project).
5. Demonstrate a range of practical skills in the use of state-of-the-art professional verification tools and environments.
6. Document verification completion criteria, monitor progress, determine verification effectiveness and assess when the project can be signed off.

https://www.bristol.ac.uk/unit-programme-catalogue/UnitDetails.jsa?ayrCode=24%2F25&unitCode=COMS30026

Design Verification Assessment

- For students taking this unit with the **Topics in Computer Science (MINOR)** examination unit, it will contribute 50% towards the 20CP Topics in Computer Science exam, (equivalent to 1 hour of exam time) that will be sat during the winter examination period. This closed-book exam will assess Learning Outcomes 1, 2, and 3.

- **For students taking this unit as a 20CP MAJOR choice, there will be two elements of assessment:**
  - A mid-term in-class written test that will assess Learning Outcomes 1, 2 and 3 (worth 30% of the unit)
  - An end-of-term practical assignment (plan, execute and document a verification activity) taking place during Weeks 9-11) that will assess Learning Outcomes 4, 5 and 6 (worth 70% of the unit)

TABLE 1: Generic Marking Criteria mapped against the three marking scales

Grade	0-20 point scale	0-100 point scale	Criteria to be satisfied
A	20 19 18	100 94 89	➢ Work would be worthy of dissemination under appropriate conditions. ➢ Mastery of advanced methods and techniques at a level beyond that explicitly taught. ➢ Ability to synthesise and employ in an original way ideas from across the subject. ➢ In group work, there is evidence of an outstanding individual contribution. ➢ Excellent presentation. ➢ Outstanding command of critical analysis and judgement.
	17 16 15	83 78 72	➢ Excellent range and depth of attainment of intended learning outcomes. ➢ Mastery of a wide range of methods and techniques. ➢ Evidence of study and originality clearly beyond the bounds of what has been taught. ➢ In group work, there is evidence of an excellent individual contribution. ➢ Excellent presentation. ➢ Able to display a command of critical analysis and judgement.
B	14 13 12	68 65 62	➢ Attained all the intended learning outcomes for a unit. ➢ Able to use well a range of methods and techniques to come to conclusions. ➢ Evidence of study, comprehension, and synthesis beyond the bounds of what has been explicitly taught. ➢ Very good presentation of material. ➢ Able to employ critical analysis and judgement. ➢ Where group work is involved there is evidence of a productive individual contribution.
C	11 10 9	58 55 52	➢ Some limitations in attainment of learning objectives but has managed to grasp most of them. ➢ Able to use most of the methods and techniques taught. ➢ Evidence of study and comprehension of what has been taught ➢ Adequate presentation of material. ➢ Some grasp of issues and concepts underlying the techniques and material taught. ➢ Where group work is involved there is evidence of a positive individual contribution.
D	8 7	48 45	➢ Limited attainment of intended learning outcomes. ➢ Able to use a proportion of the basic methods and techniques taught. ➢ Evidence of study and comprehension of what has been taught, but grasp insecure. ➢ Poorly presented. ➢ Some grasp of the issues and concepts underlying the techniques and material taught, but weak and incomplete.
E	6	42	
	5	35	➢ Attainment of only a minority of the learning outcomes. ➢ Able to demonstrate a clear but limited use of some of the basic methods and techniques taught. ➢ Weak and incomplete grasp of what has been taught. ➢ Deficient understanding of the issues and concepts underlying the techniques and material taught.
	1 - 4	7 - 29	➢ Attainment of nearly all the intended learning outcomes deficient. ➢ Lack of ability to use at all or the right methods and techniques taught. ➢ Inadequately and incoherently presented. ➢ Wholly deficient grasp of what has been taught. ➢ Lack of understanding of the issues and concepts underlying the techniques and material taught.
0	0	0	➢ No significant assessable material, absent, or assessment missing a "must pass" component.

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Literature and Study Resources

- **Writing Testbenches: Functional Verification of HDL Models** by Janick Bergeron. Second Edition, Kluwer, 2003.
- **Comprehensive Functional Verification** by Bruce Wile, John Goss and Wolfgang Roesner. Elsevier, 2005.
- verificationacademy.com
- **In addition:**
  - Lecture slides on github unit web page
  - Supplementary literature and activities on gihub unit web page

[**Credits:** Parts of the lecture notes contain material from the book “Comprehensive Functional Verification” by Bruce Wile etal, the book ”Writing Testbenches: Functional Verification of HDL Models” by Janick Bergeron, the book ”The Verilog Hardware Description Language” by Donald Thomas and from lecture slides developed at IBM (by Avi Ziv and Jaron Wolfstal), the University of Pittsburgh, Penn State University, North Carolina State University and Ohio State University. The HDL for the assignments has been developed at IBM.]

Questions

https://www.bristol.ac.uk/tsl