COMS30026 Design Verification

Functional Formal Verification

Kerstin Eder

Trustworthy Systems Laboratory
https://www.bristol.ac.uk/engineering/research/trustworthy-systems-laboratory/

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Functional Verification Approaches

- Verification
  - Static
    - Reviews
    - Code Analysis
      - Linters
  - Dynamic
    - Simulation
    - Prototyping
      - Silicon
      - FPGA

- Formal
  - Equivalence Checking
  - Property Checking
  - Theorem Proving
  - Emulation
Functional Verification Approaches

Verification

Static
- Reviews
- Code Analysis
  - Linters
- Formal
  - Equivalence Checking
  - Property Checking
  - Theorem Proving

Dynamic
- Prototyping
  - Silicon
  - FPGA
  - Emulation

Hybrid
- Dynamic Formal
Formal Property Checking

Properties of a design (aka assertions) are formally proven or disproved.

- Used to complement simulation-based verification.
- Usually employed at lower levels in the design hierarchy.

Give a reconvergence model for formal property checking!

A reconvergence model is a conceptual representation of the verification process. It helps us understand what is being verified.
Reconvergence Model for Formal Property Checking
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- Properties are derived from the specification. (interpretation step)
- Properties are expressed as formulae in some (temporal) logic.

![Diagram showing the process from Specification to RTL Coding through Interpretation]

- Specification
- Interpretation
- RTL Coding
- RTL
Reconvergence Model for Formal Property Checking

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![Diagram showing the reconvergence model for formal property checking]

- **Specification** → **Interpretation** → **Property Formalization** → **Properties (Assertions)** → **RTL Coding** → **RTL**

**under env_constraint if condition then expectation**

**pre-condition** → **post-condition**
Reconvergence Model for Formal Property Checking

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- Properties are expressed as formulae in some (temporal) logic.
- Checking is typically performed on a Finite State Machine model of the design.
  - This may be an FSM model of the RTL (as shown in the example).
Reconvergence Model for Formal Property Checking

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- **Properties** are expressed as formulae in some (temporal) logic.
- **Checking** is typically performed on a Finite State Machine model of the design.
  - This may be the **RTL** (as shown in the example).

There are also Model Checkers for software, e.g. C, C++ and Java.

Overview of Formal Property Checking

- Property Checking is the **most common form** of high-level formal verification used in practice.
- Property checking is **fully automatic.** ✓
  - Requires the properties to be written.
- It performs **exhaustive verification** of the design **wrt the specified properties.**
- It provides **proofs** and can demonstrate the **absence of bugs.**
- A **counterexample** is presented for failed properties.
- Frequently used for critical, well specified parts of the design, e.g. cache coherence protocols, bus protocols, interrupt controllers, interfaces
Scalability of Formal Verification

Due to the fact that formal verification is exhaustive, formal methods can suffer from capacity limits.

Symbolic Model Checking: $10^{20}$ States and Beyond*

J. R. Burch, E. M. Clarke, and K. L. McMillan

School of Computer Science, Carnegie Mellon University, Pittsburgh, Pennsylvania 15213

AND

D. L. Dill and L. J. Hwang

Stanford University, Stanford, California 94305

Many different methods have been devised for automatically verifying finite state systems by examining state-graph models of system behavior. These methods all depend on decision procedures that explicitly represent the state space using a list or a table that grows in proportion to the number of states. We describe a general method that represents the state space symbolically instead of explicitly. The generality of our method comes from using a dialect of the Mu-Calculus as the primary specification language. We describe a model checking algorithm for Mu-Calculus formulas that uses Bryant’s Binary Decision Diagrams (Bryant, R. E., 1986, IEEE Trans. Comput. C-35) to represent relations and formulas. We then show how our new Mu-Calculus model checking algorithm can be used to derive efficient decision procedures for CTL model checking, satisfiability of linear-time temporal logic formulas, strong and weak observational equivalence of finite transition systems, and language containment for finite $\omega$-automata. The fixed point computations for each decision procedure are sometimes complex, but can be concisely expressed in the Mu-Calculus. We illustrate the practicality of our approach to symbolic model checking by discussing how it can be used to verify a simple synchronous pipeline circuit.

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How big is exhaustive?

- Consider simulating a typical CPU design
  - 500k gates, 20k DFFs, 500 inputs
  - 70 billion simulation cycles,
    running on 200 linux boxes for a week
  - How big: $2^{36}$ cycles
How big is exhaustive?

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- Consider formally verifying this design
  - Input sequences: cycles $2^{(\text{inputs}+\text{state})} = 2^{20500}$
  - What about X’s: $2^{15000}$ (5,000 X-assignments + 10,000 non-reset DFFs)
  - How big: $2^{20500}$ cycles ($2^{15000}$ combinations of X is not significant here!)
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- These are a big numbers!
  - Cycles to simulate the 500k gate CPU design: $2^{36}$ (70 billion)
  - Cycles to formally verify a 32-bit adder: $2^{64}$ (18 billion billion)
  - Number of stars in universe: $2^{74}$ ($10^{22}$)
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- These are big numbers!
  - Cycles to simulate the 500k gate CPU design: \(2^{36}\) (70 billion)
  - Cycles to formally verify a 32-bit adder: \(2^{64}\) (18 billion billion)
  - Number of stars in universe: \(2^{74}\) (\(10^{22}\))
  - Number of atoms in the universe: \(2^{260}\) (\(10^{78}\))
  - Possible X combinations in 500k gate design: \(2^{15000}\) (\(10^{4515} \times 3\))
  - Cycles to formally verify the 500k gate design: \(2^{20500}\) (\(10^{6171}\))
Managing complexity in FV

- There are tried and trusted techniques to overcome the capacity limitations of FV:
  - Start with narrow focus on block level, work up towards higher levels in the design hierarchy turning proven assertions into assumptions
  - Restrict property checking to work over finite small time windows.
  - Limit environment behaviour by strengthening constraints.
  - Case splits over a set of properties, partitioning and black boxing.
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Simulation vs Formal Verification

Only selected parts of the design can be covered during simulation.

Simulation vs Formal Verification

Challenge 1:
Specify properties to cover the entire design.

Challenge 2:
Prove all these properties.

Only selected parts of the design can be covered during simulation.

Naïve interpretation of exhaustive formal verification:

Verify ALL properties.

Simulation vs Formal Verification

In practice, completeness issues and capacity limits restrict formal verification to selected parts of the design.

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Only selected parts of the design can be covered during simulation.

Verify ALL properties.

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Challenge 2:
Prove all these properties.

In practice, completeness issues and capacity limits restrict formal verification to selected parts of the design.

Outcomes of Formal Property Checking

- Formulate Property
  - Invoke Property Checker
    - Property proven
      - Vacuity check
        - Property is trivially true
          - Bug in Property
        - Property is non-trivially true
          - DUV satisfies Property
    - Property fails
      - Counterexample (CE)
        - Unreachable
          - No reachable other CE exists
            - Bug in Property
          - Reachable other CE exists
            - DUV bug detected
        - Reachable
          - DUV bug detected
Outcomes of Formal Property Checking

- Formulate Property
  - Invoke Property Checker
    - Property proven
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        - Property is trivially true
          - Bug in Property
        - Property is non-trivially true
          - DUV satisfies Property
    - Property fails
      - Counterexample (CE)
        - Unreachable
          - Other cases exist
            - DUV bug detected
        - Reachable
          - DUV bug detected

Specify environment constraints for proof.

Correctness of proof relies on correctness of the environment constraints.
Outcomes of Formal Property Checking

- **Formulate Property**
  - **Invoke Property Checker**
  - **Property proven**
  - **Property fails**
  - **Vacuity check**
    - **Bug in Property**
    - **Property is trivially true**
    - **Property is non-trivially true**
  - **DUV satisfies Property**
  - **Counterexample (CE)**
    - **Unreachable**
      - **Correctness of proof relies on correctness of the environment constraints.**
    - **Reachable**
      - **DUV bug detected**
  - **Bug in Property**
  - **DUV bug detected**

Most common mistake, restrict input space so much that property becomes trivially true.

Specify environment constraints for proof.
Outcomes of Formal Property Checking

1. Formulate Property
2. Invoke Property Checker
3. Property proven
4. Property is trivially true
5. DUV satisfies Property
6. Bug in Property
7. Property fails
8. Property is non-trivially true
9. Under-constrained properties may lead to unreachable counterexamples.
10. Unreachable
11. No reachable other CE exists
12. Reachable other CE exists
13. Reachable
14. DUV bug detected
15. Counterexample (CE)
16. Bug in Property
17. DUV bug detected

- Most common mistake, restrict input space so much that property becomes trivially true.
- Specify environment constraints for proof.
How do you know you’ve encoded the property right?

- Keep properties and sequences **simple**; build complex properties from simple, short properties.
- **Peer review** properties you write.
- **Know what to expect**, e.g. create failing conditions.
- If the property fails (when you expect it to succeed), then **investigate the counterexample:**
  - Is it reachable or not?

- But if the property succeeds, how do you know whether you’ve encoded the property right?
HANDS-ON FORMAL PROPERTY CHECKING DEMO
Formal Property Checking

- Jasper DEMO
  - **DUV**: FIFO design from ABV lecture
  - Verification of selected FIFO properties from ABV
The demo session includes

- Automatic generation of basic properties using "Visualize":
  - Basic functionality of the DUV
  - Range checks of signals

- Verification of SVA properties:
  - “Empty and full are never asserted together.”
  - “After clear the FIFO is empty.”
  - “On empty after one write the FIFO is no longer empty.”

- Inspect and understand counterexamples:
  - Debug several failed properties

Note:
- Close link to coverage closure (by construction).
- Link from env_constraints to simulation assertions.
Summary

Functional Formal Verification

- Distinction between static and dynamic verification techniques
- Reconvergence model for formal verification
- What happens during formal verification
- Capacity limits and techniques to manage complexity
- Simulation vs. formal verification
- Outcomes of formal property checking
- Guidelines on writing properties
Conclusion

No single method is adequate to verify a whole design in practice.

- Carefully select the verification methods that maximize ROI for each level in the design hierarchy.
- Complement simulation with formal verification techniques to exploit the benefits and mitigate the limitations of each technique.